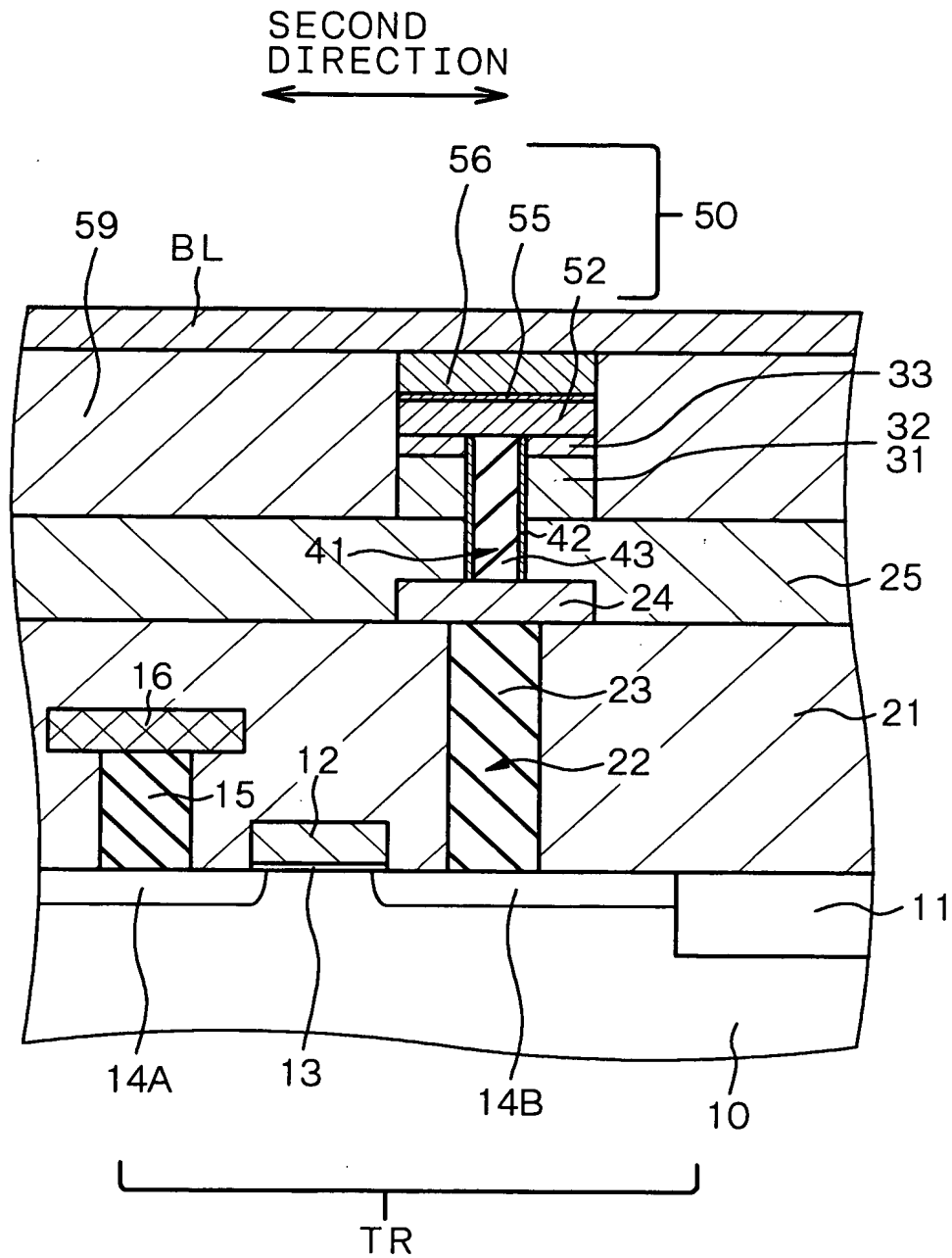
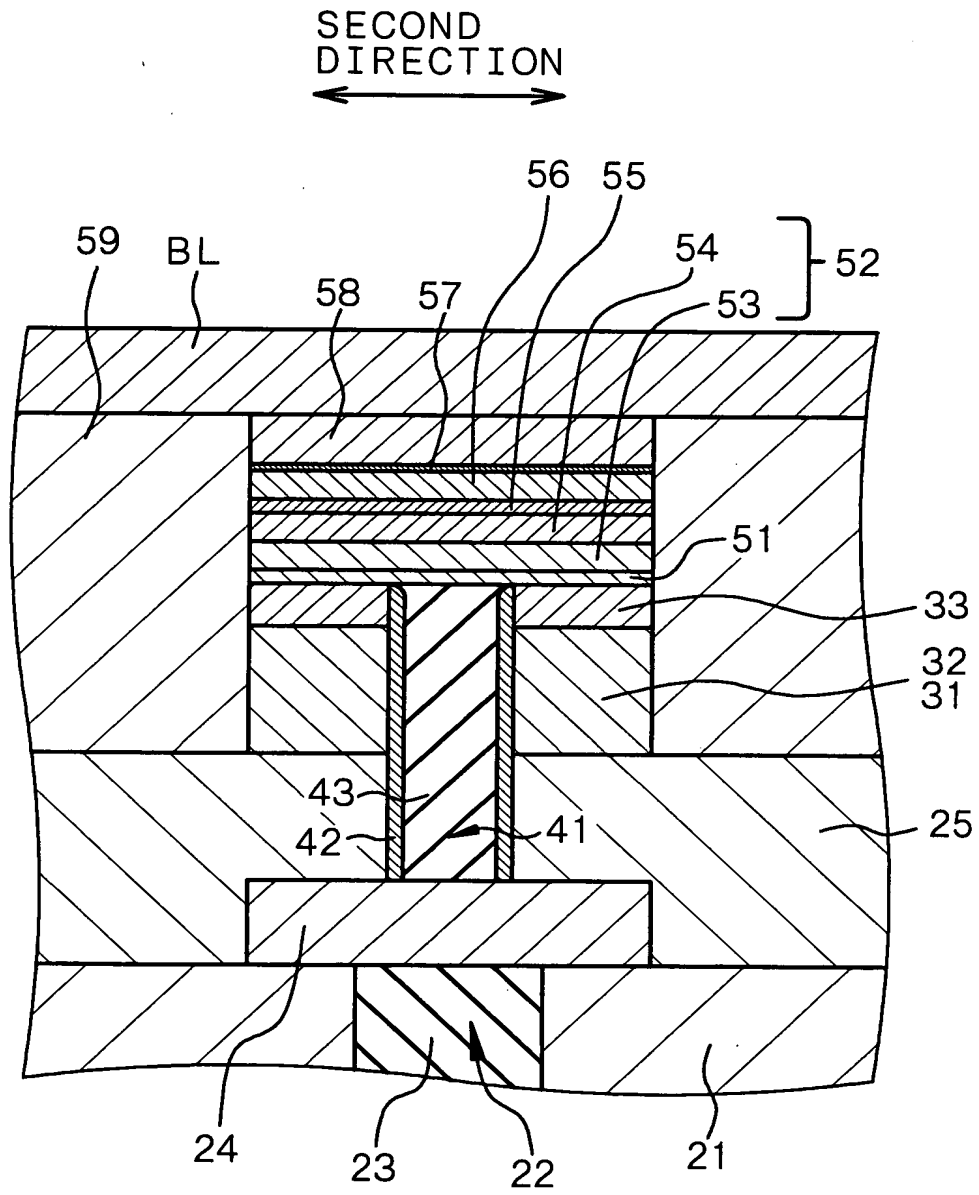


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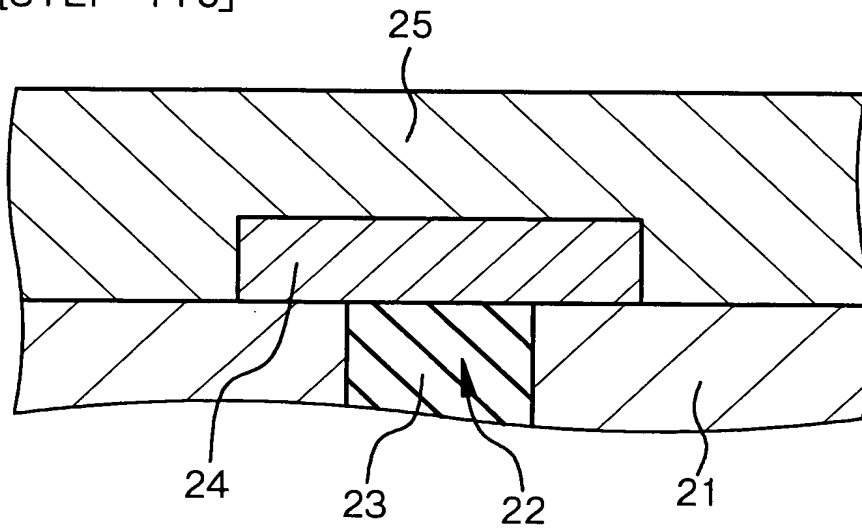
Fig. 1



*Fig. 2*

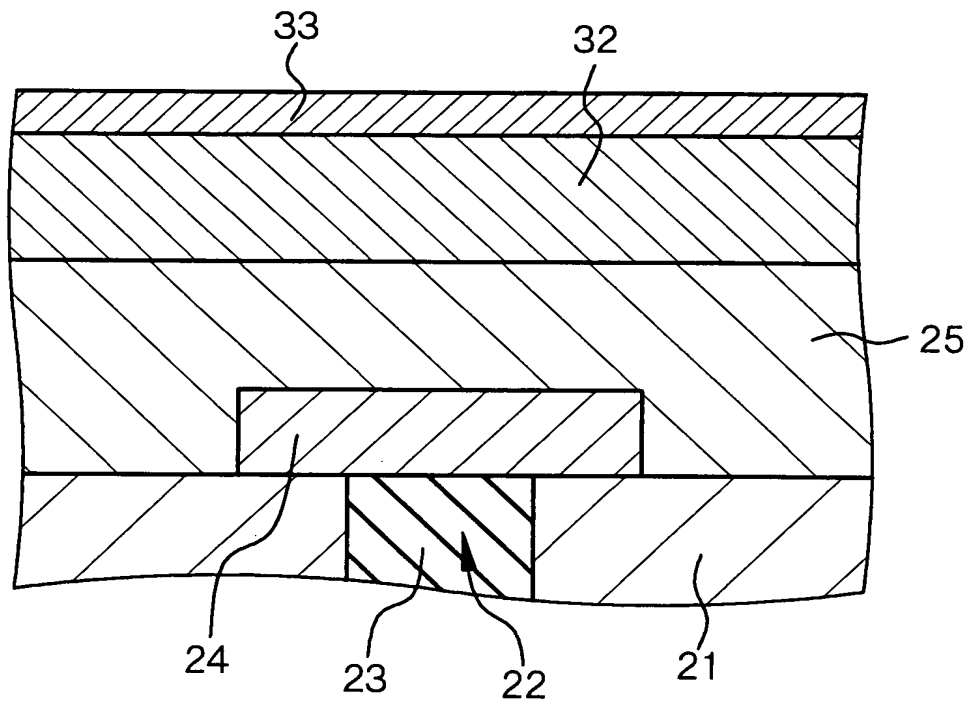
*Fig. 3A*

[STEP-115]



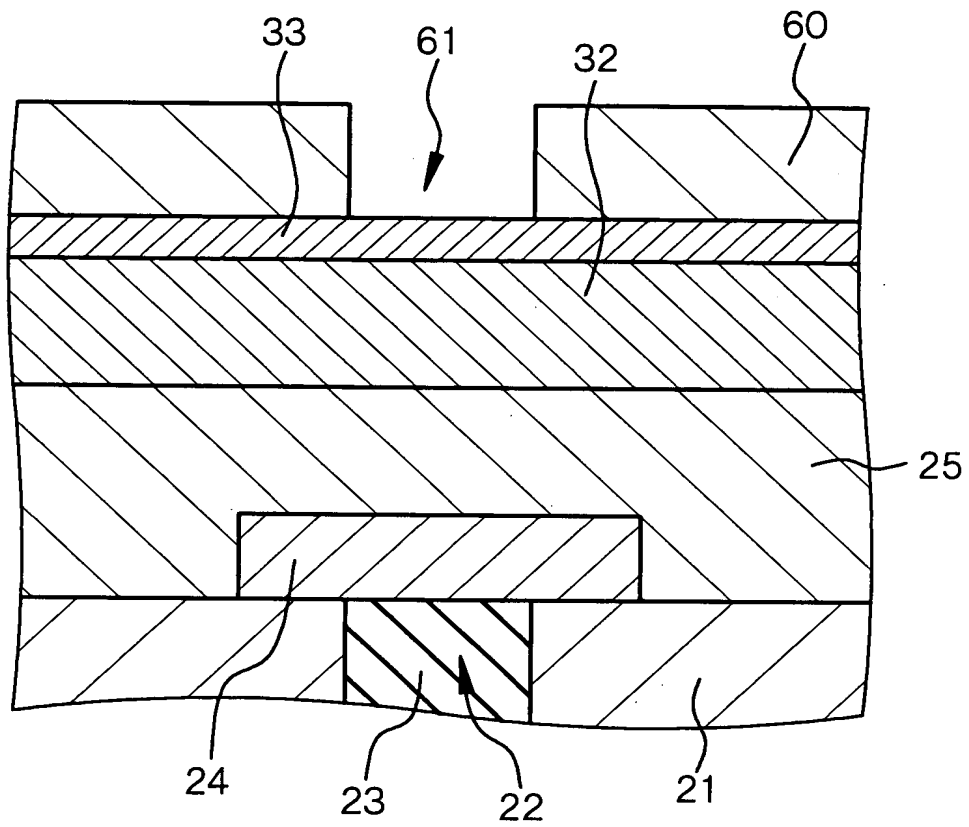
*Fig. 3B*

[STEP-120]



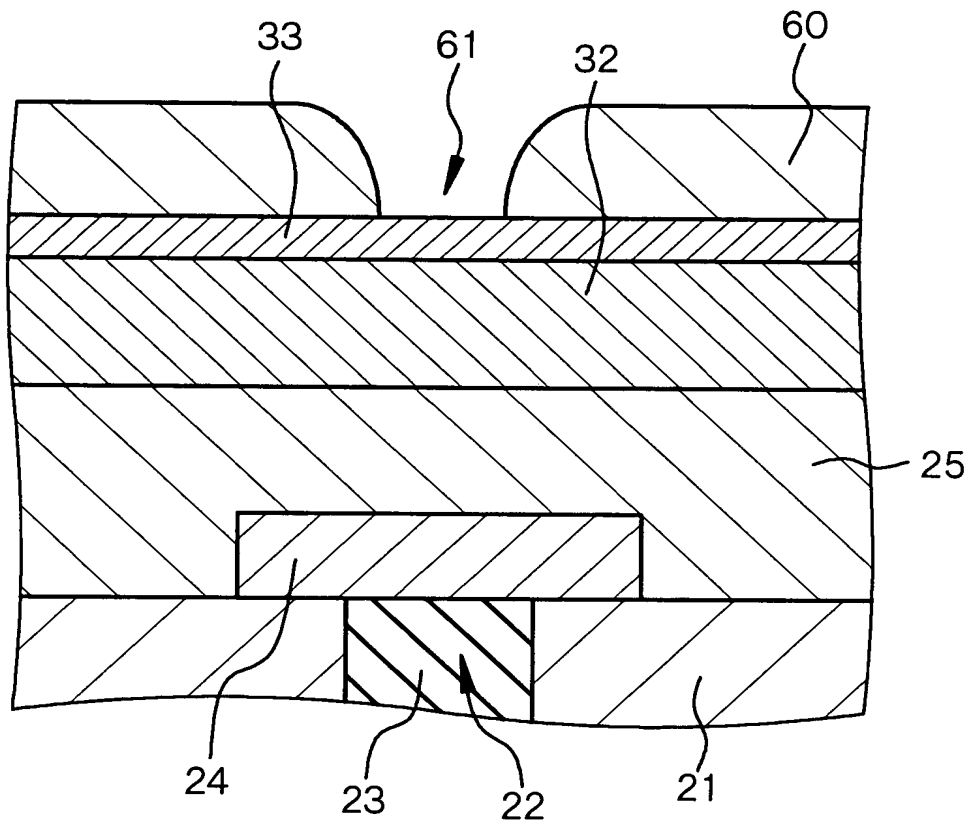
*Fig. 4*

[STEP-125]



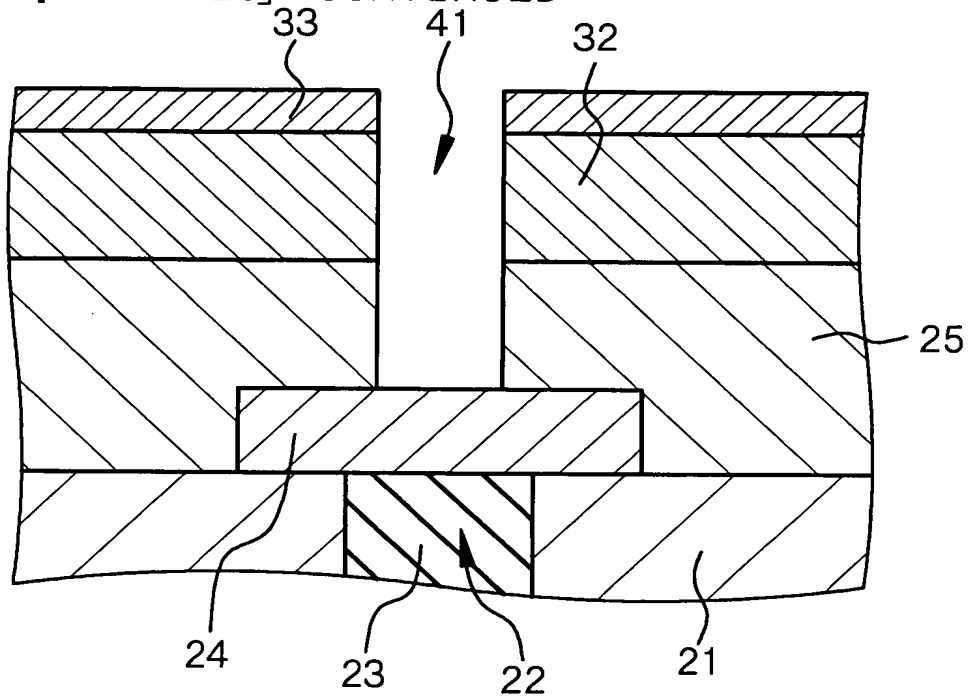
*Fig. 5*

[STEP-125] CONTINUED

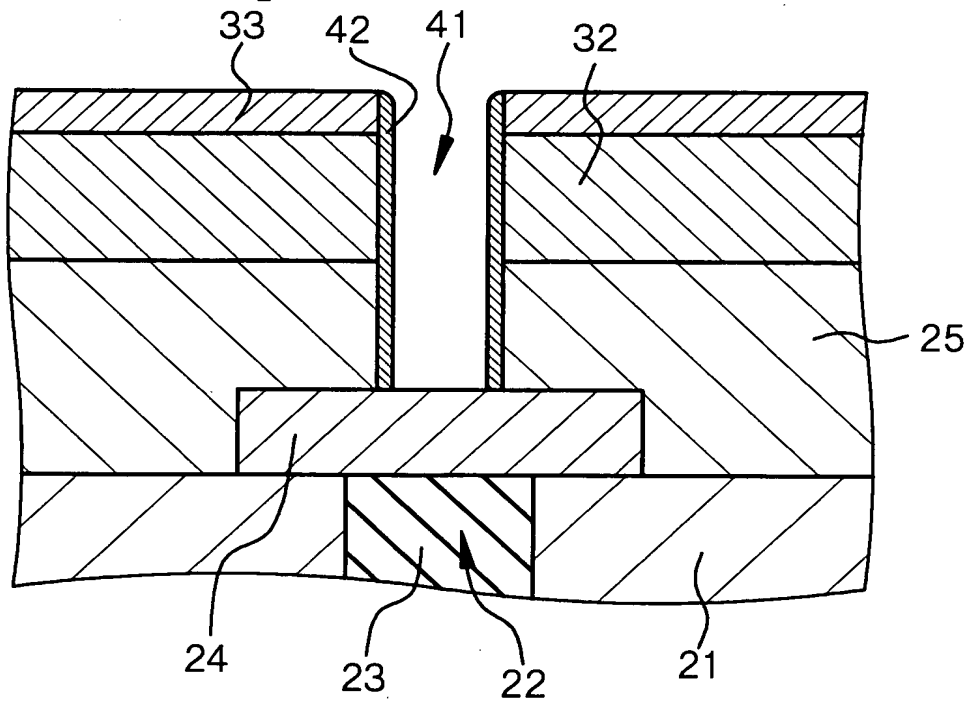


*Fig. 6A*

[STEP-125] CONTINUED

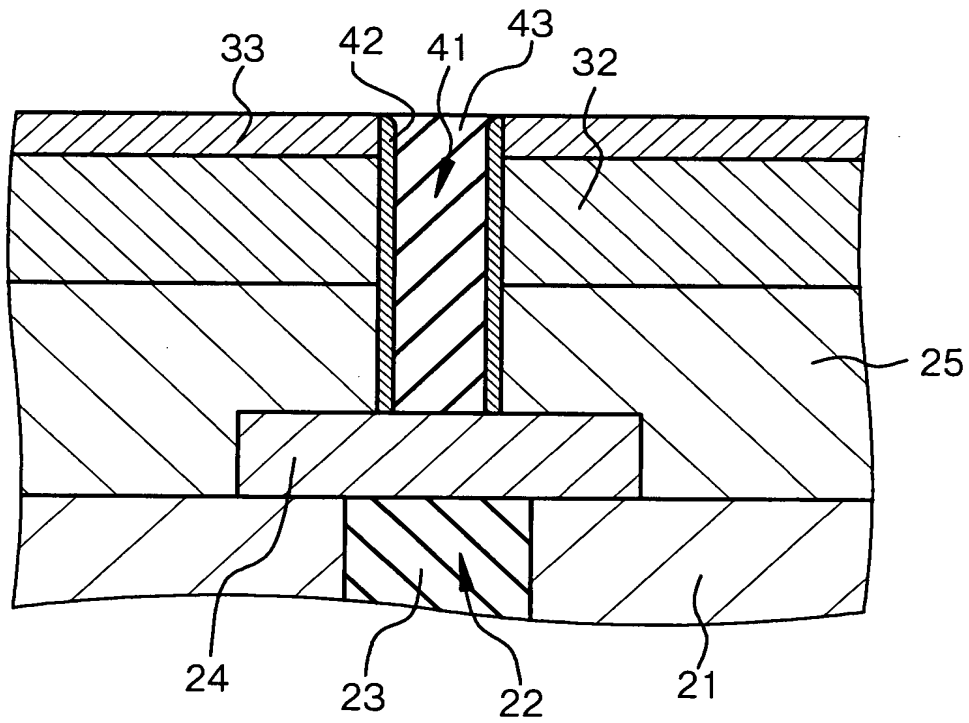
*Fig. 6B*

[STEP-125] CONTINUED



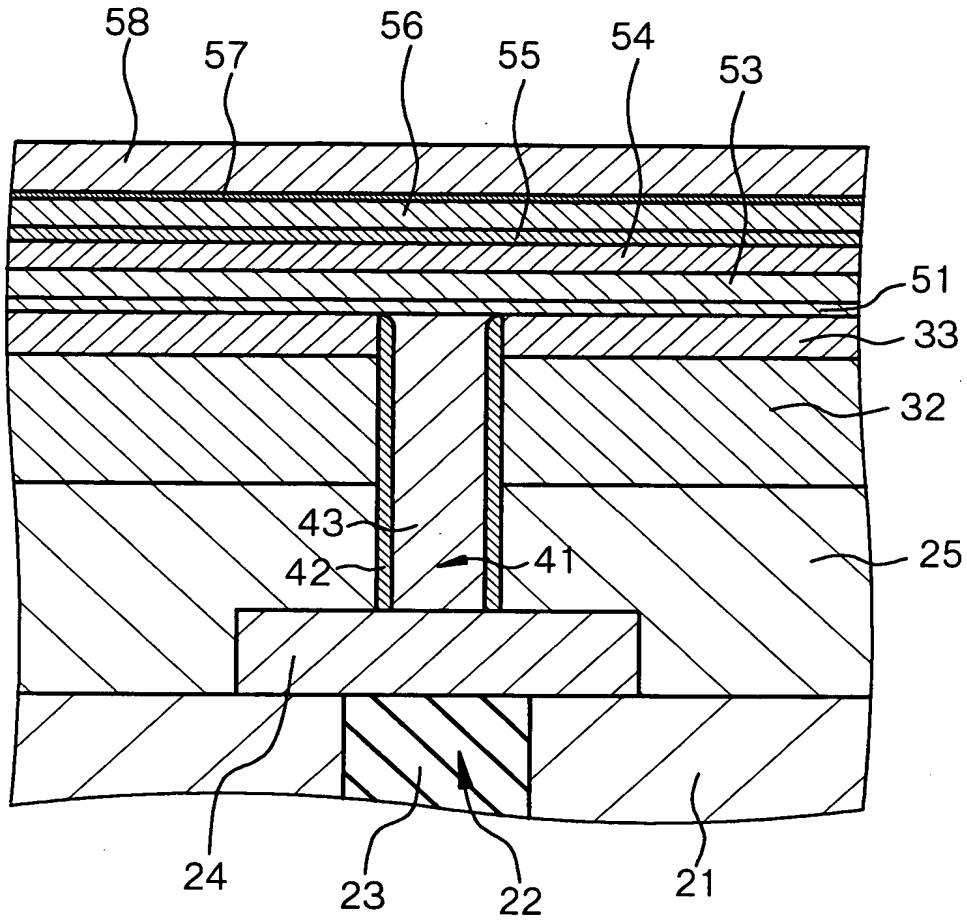
*Fig. 7*

[STEP-125] CONTINUED



*Fig. 8*

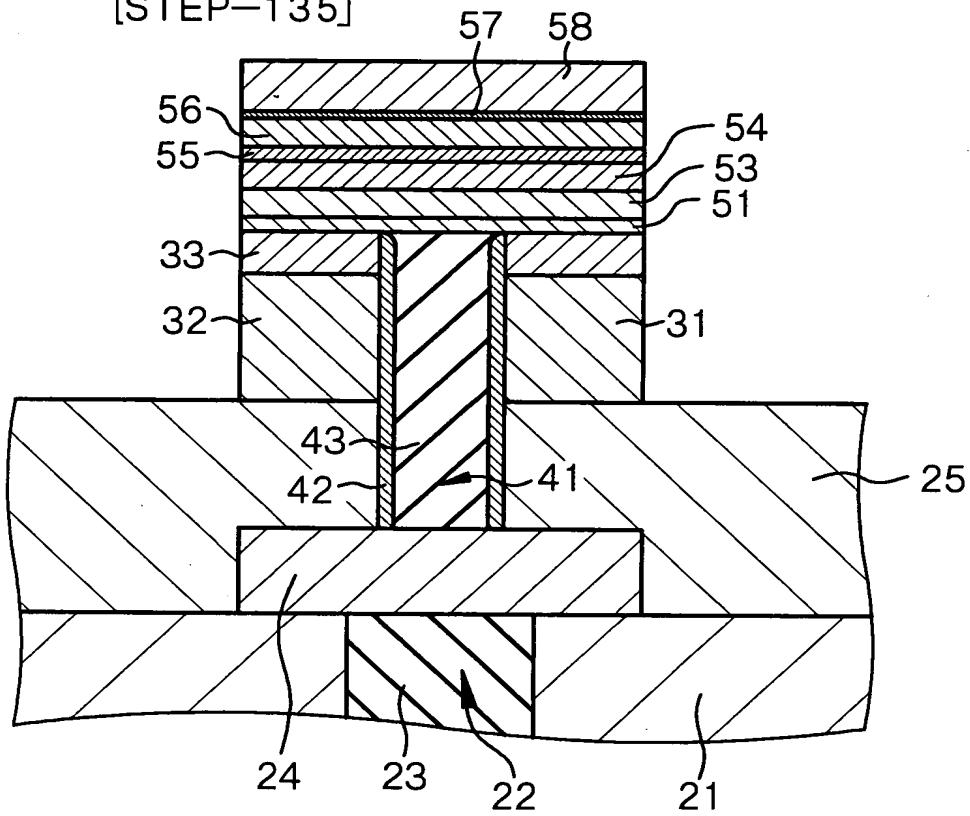
[STEP-130]



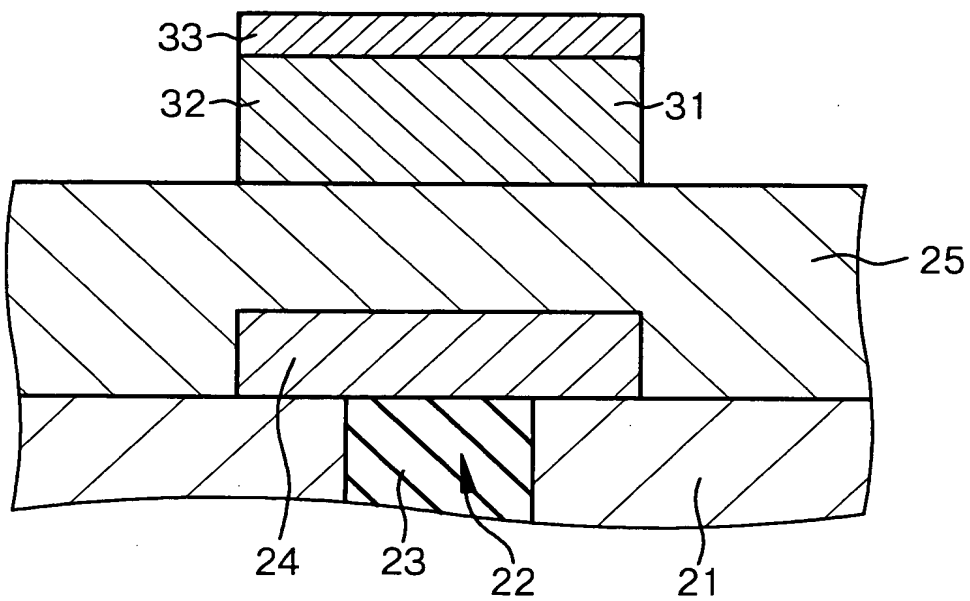


*Fig. 9A*

[STEP-135]

*Fig. 9B*

[STEP-140]



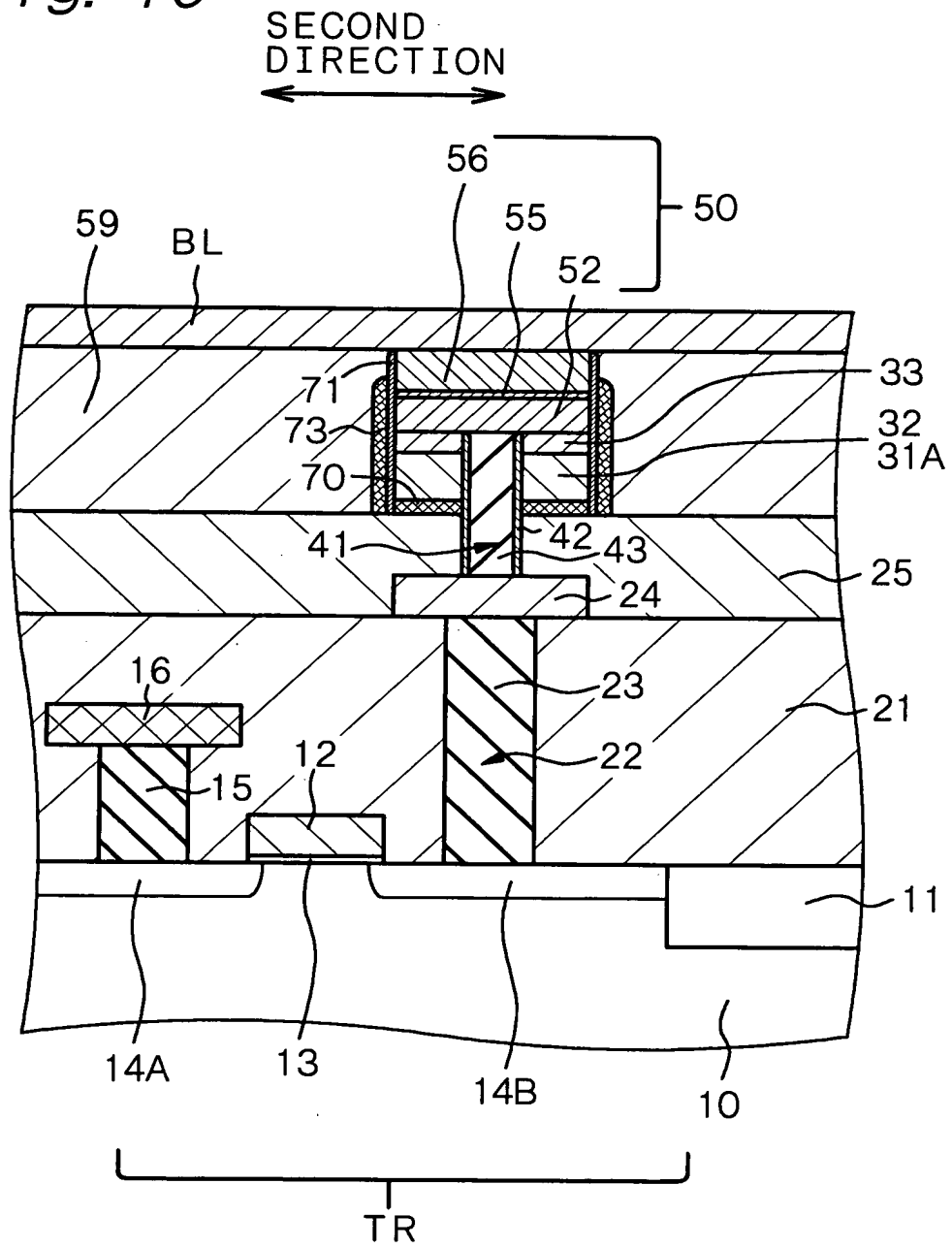
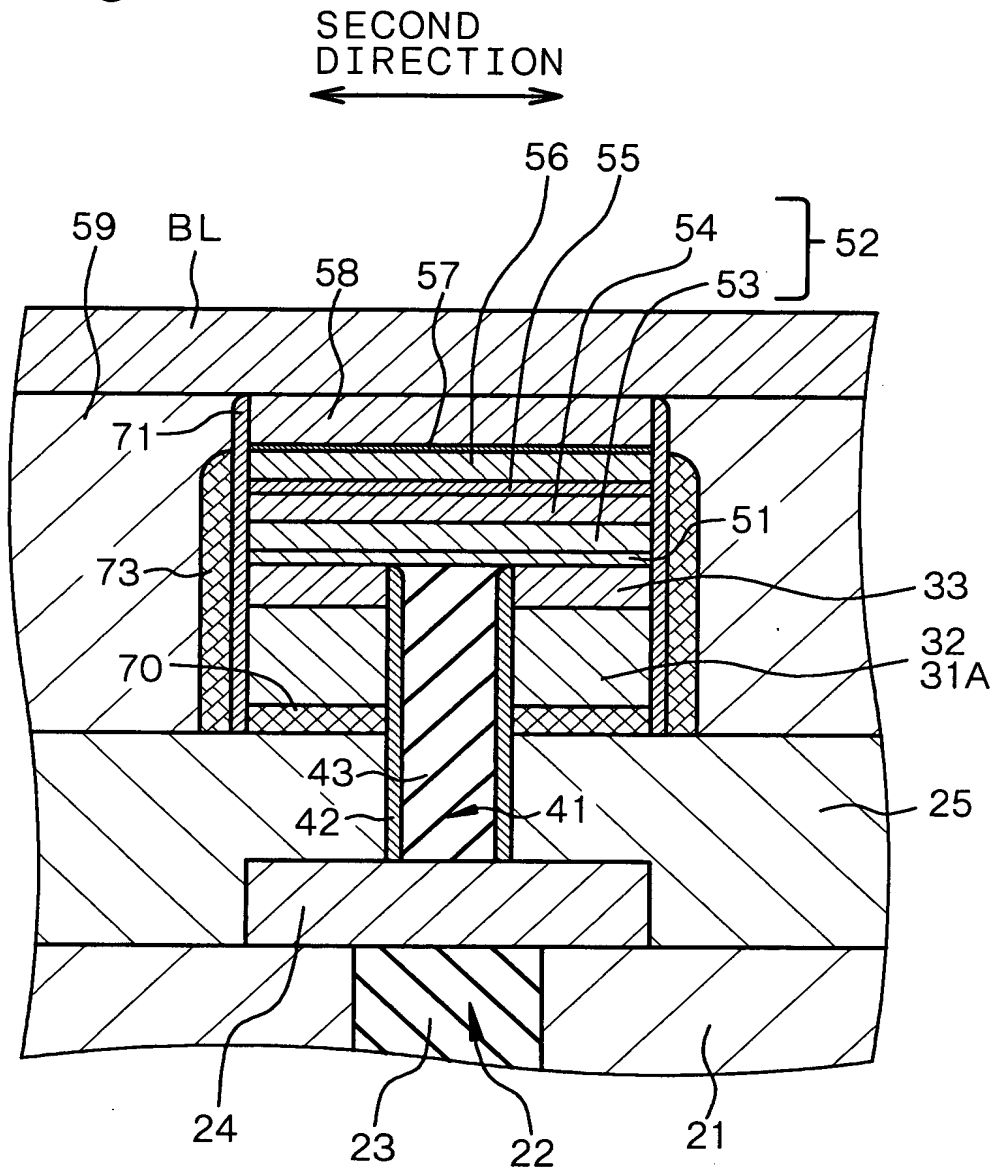
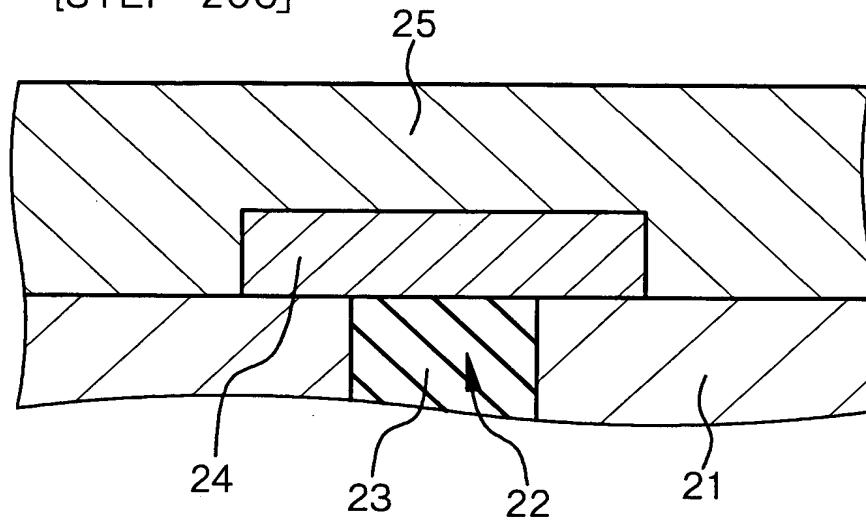
*Fig. 10*

Fig. 11



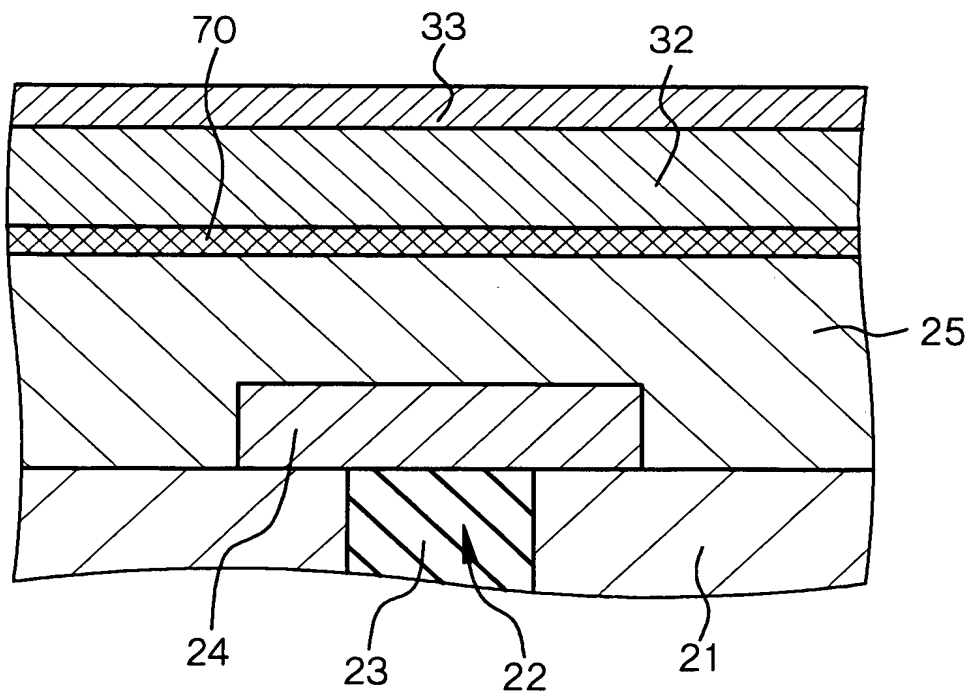
*Fig. 12A*

[STEP-200]

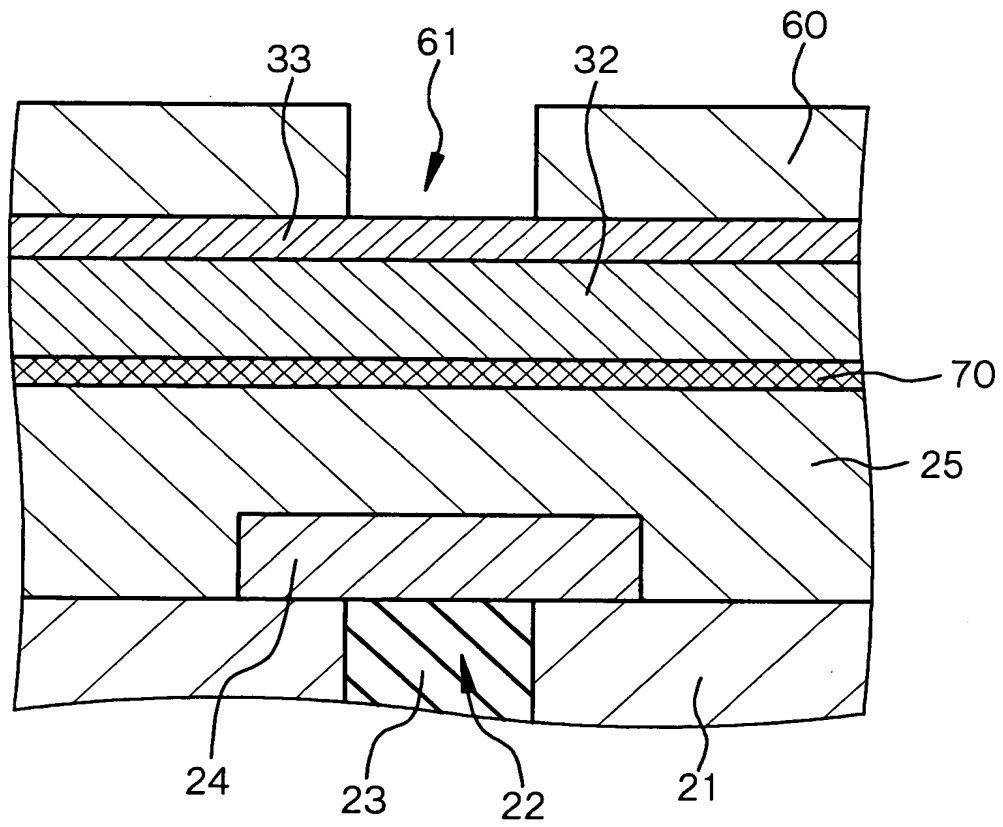


*Fig. 12B*

[STEP-205]

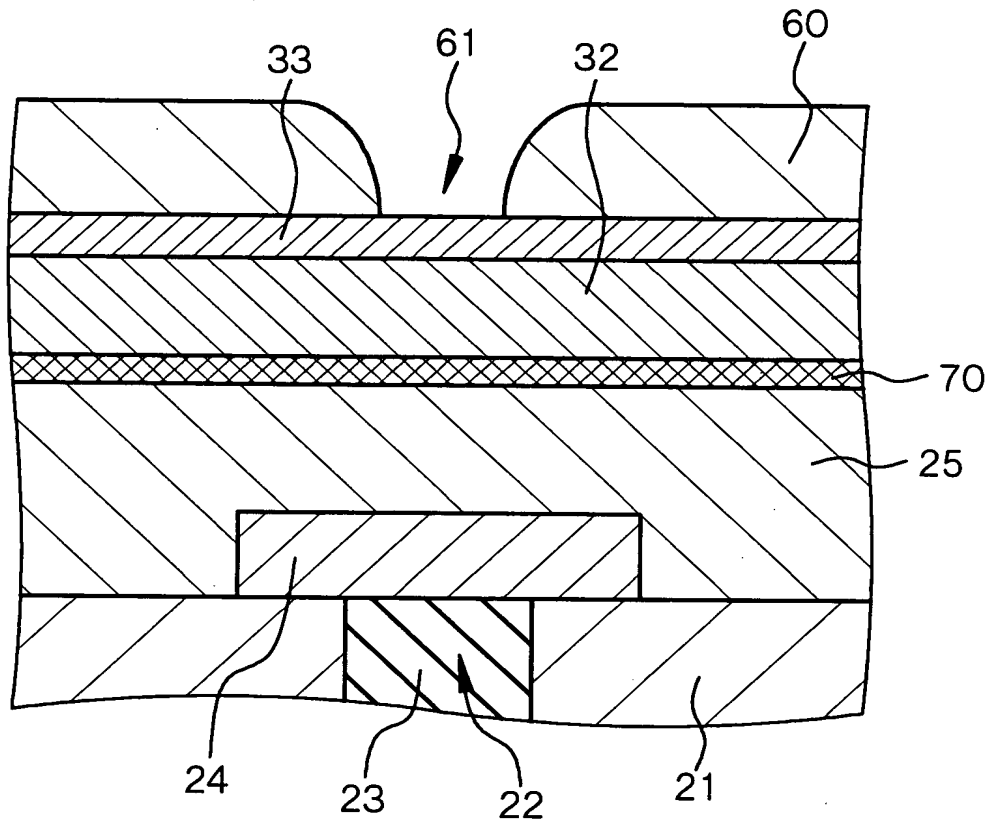


[STEP-210]



*Fig. 14*

[STEP-210] CONTINUED

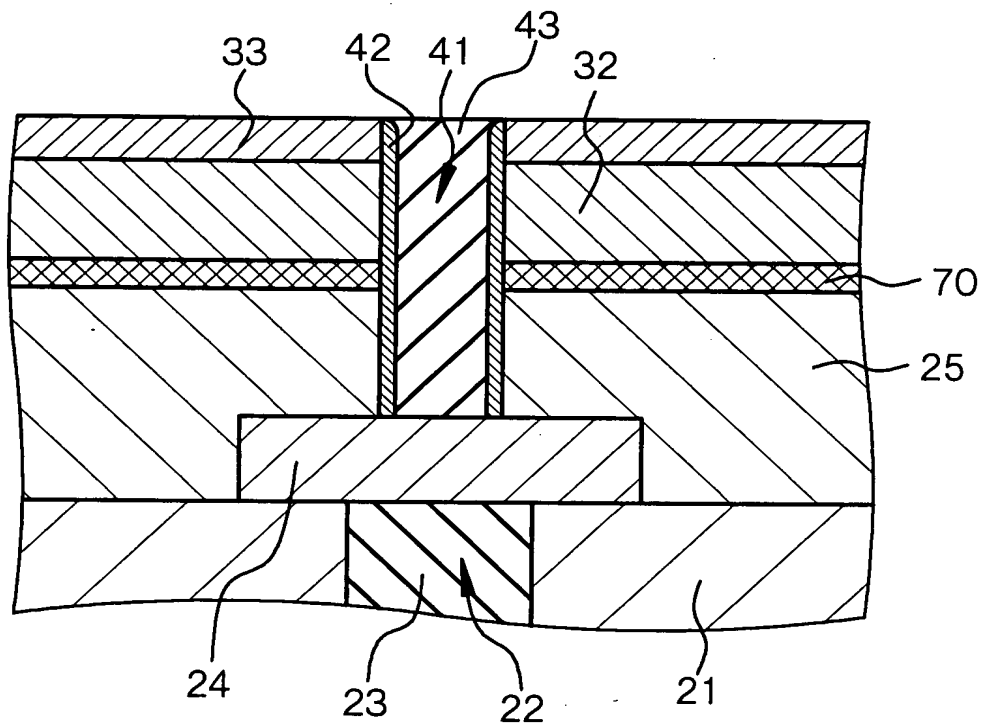


*Fig. 15B*

A cross-sectional view of a semiconductor device. The device consists of a substrate 21, a base layer 22, a patterned layer 23, and a top layer 24. A central opening is filled with a material 32, and a surrounding layer 33 is shown. A cross-hatched layer 70 is also visible. A vertical structure 41 is shown on the right side.

*Fig. 16*

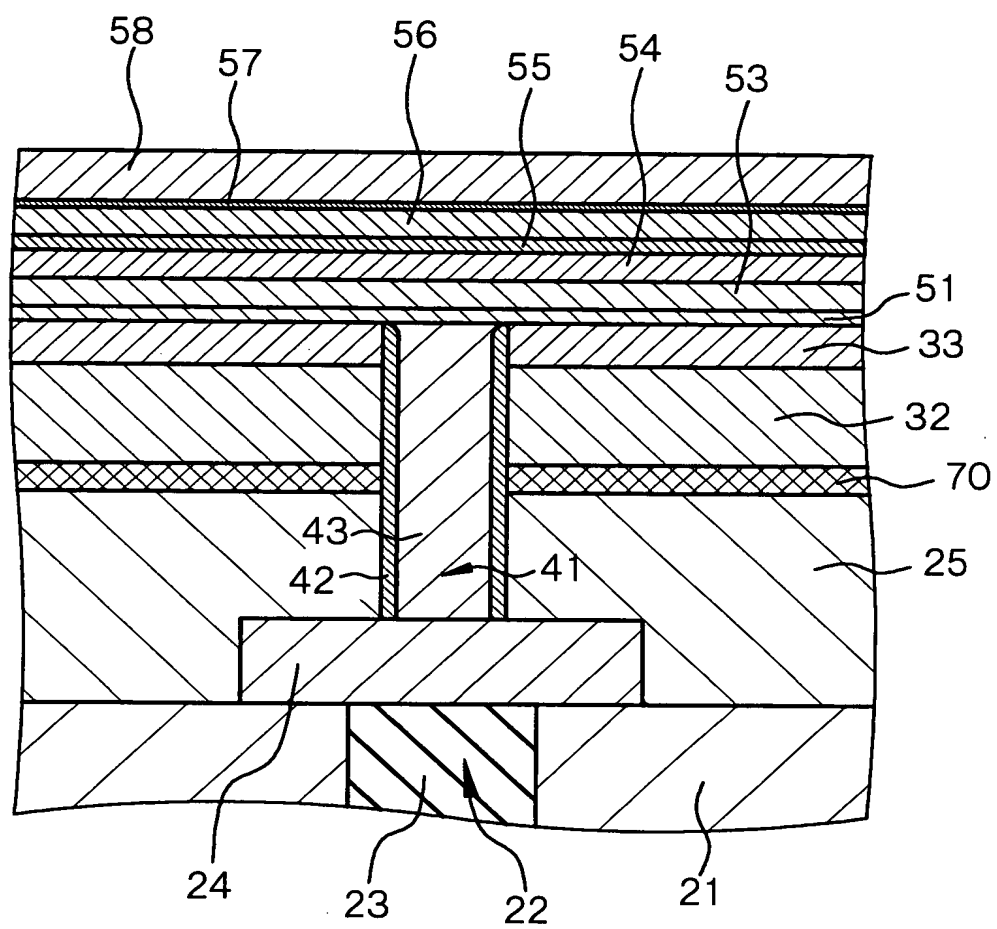
[STEP-210] CONTINUED





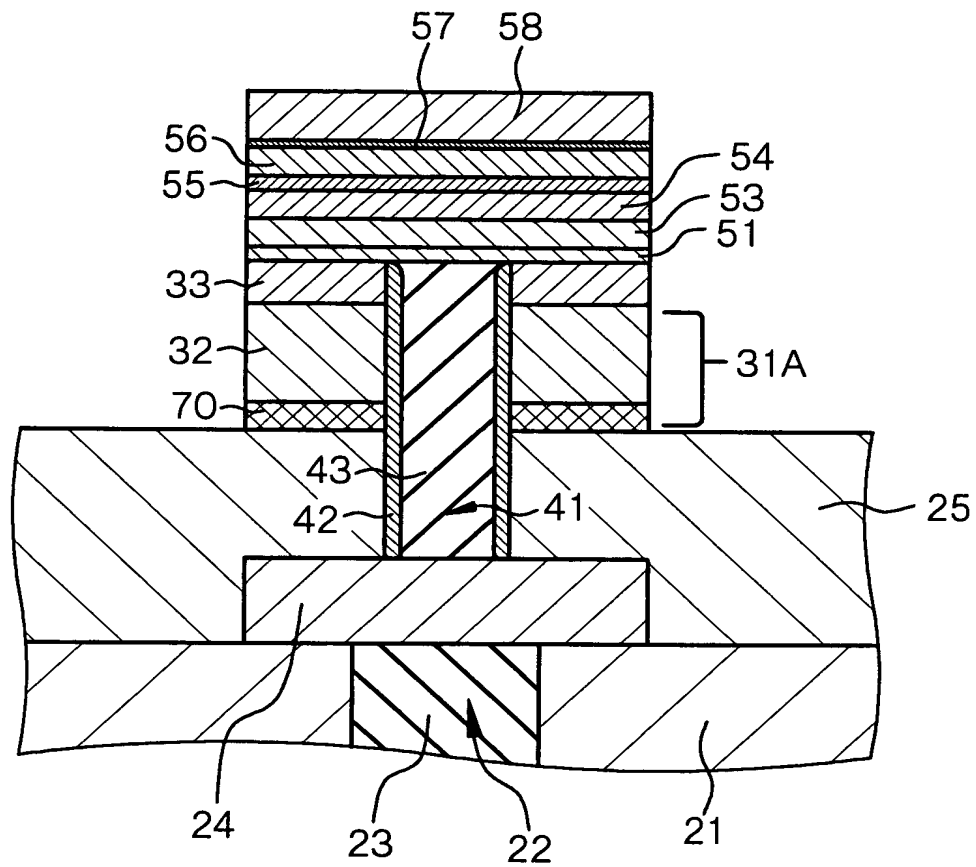
*Fig. 17*

[STEP-215]



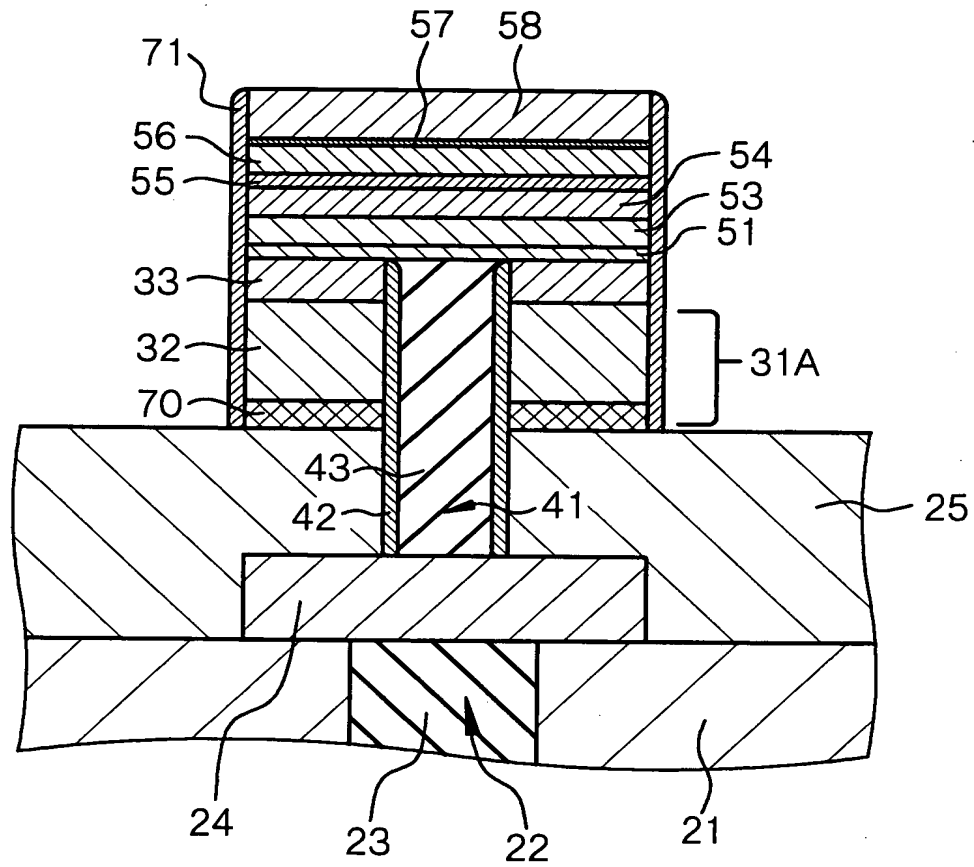
*Fig. 18*

[STEP-220]



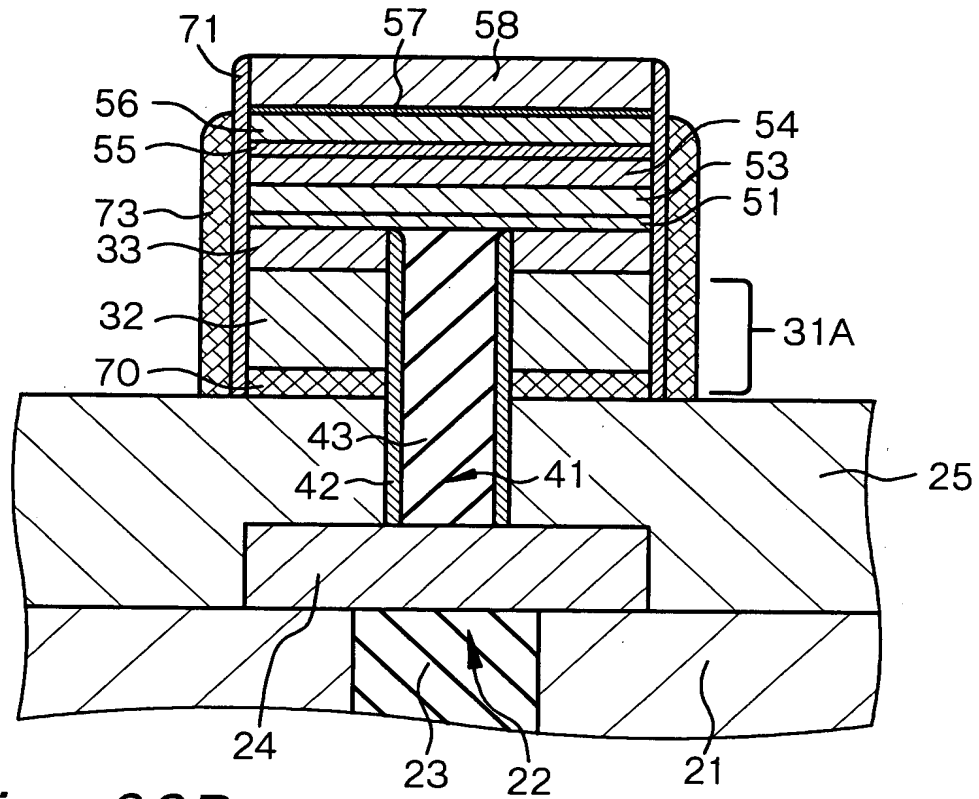
*Fig. 19*

[STEP-225]

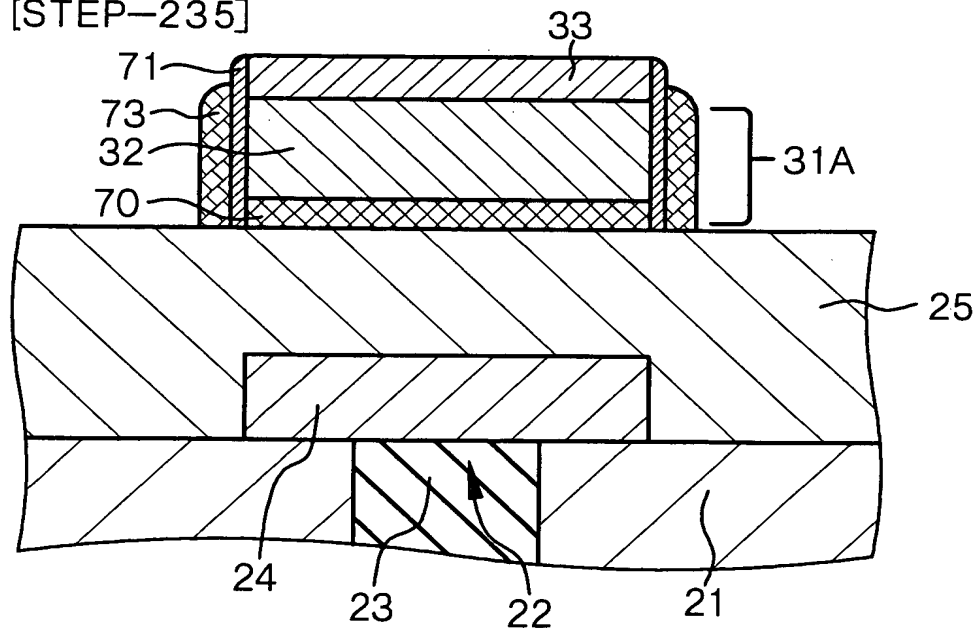


*Fig. 20A*

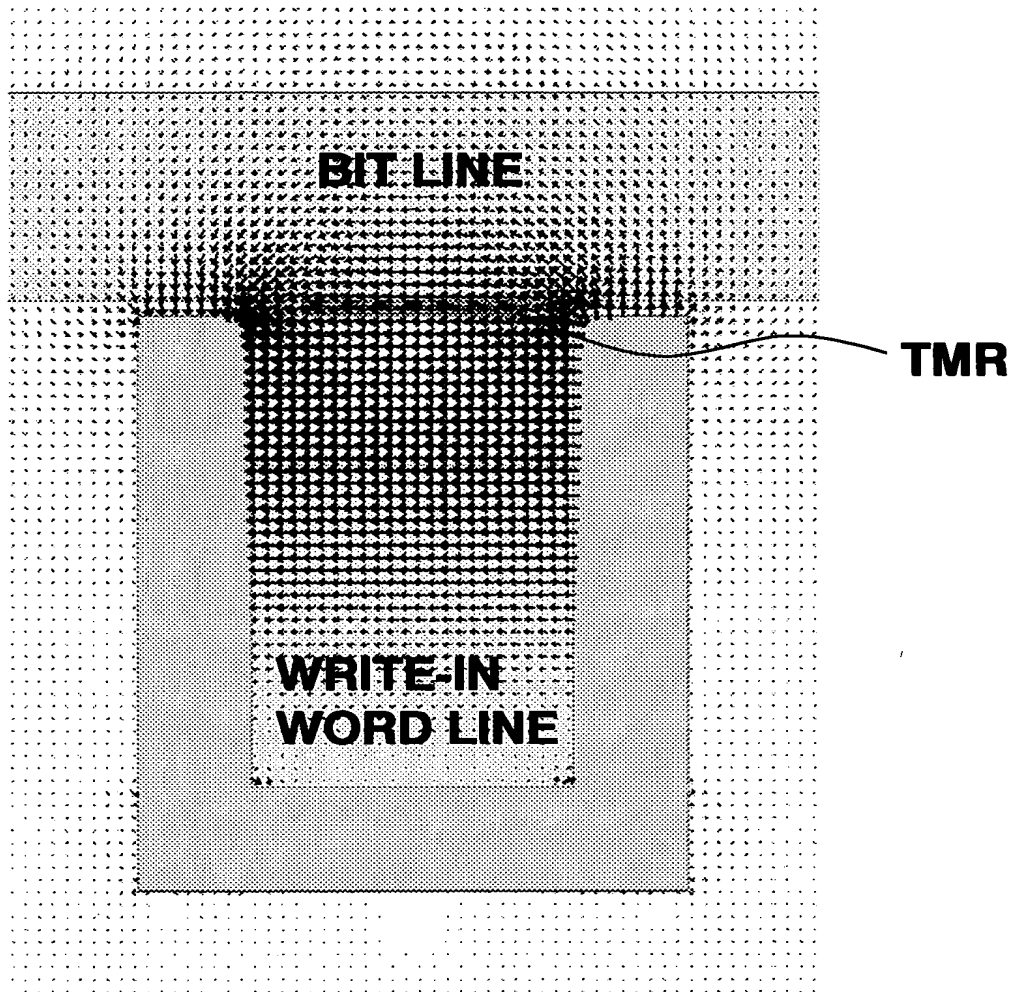
[STEP-230]

*Fig. 20B*

[STEP-235]



*Fig. 21*



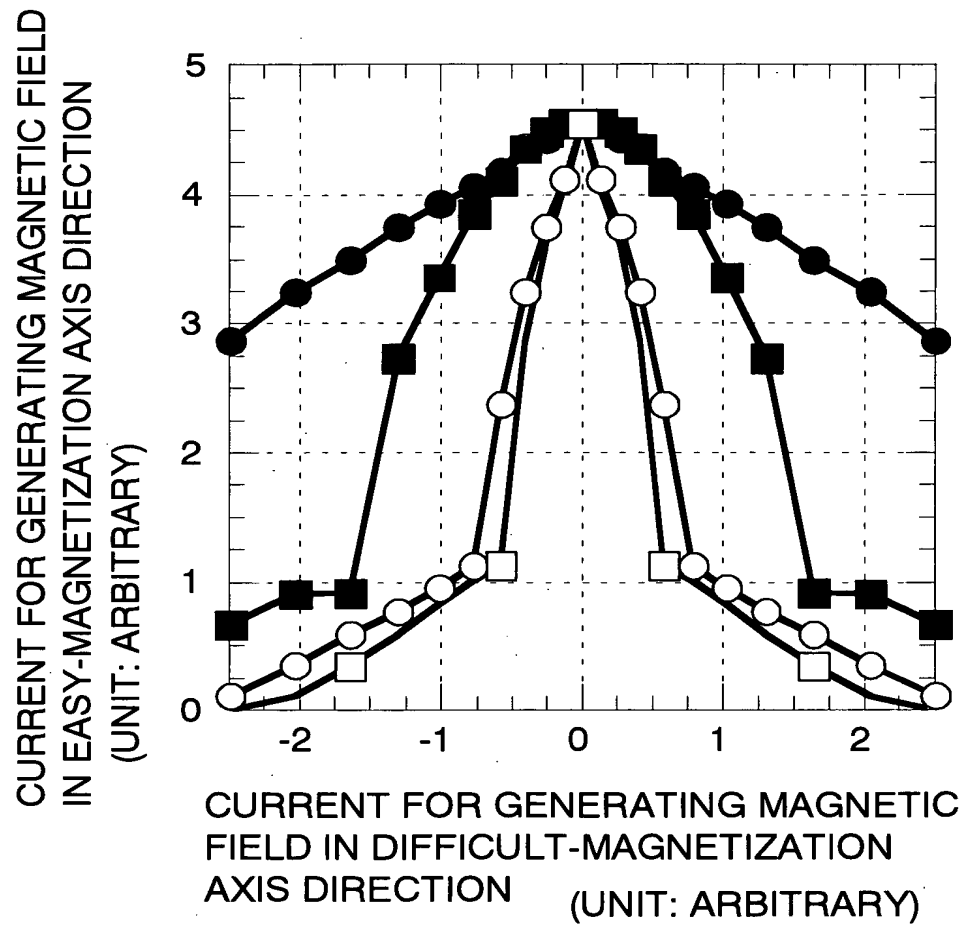
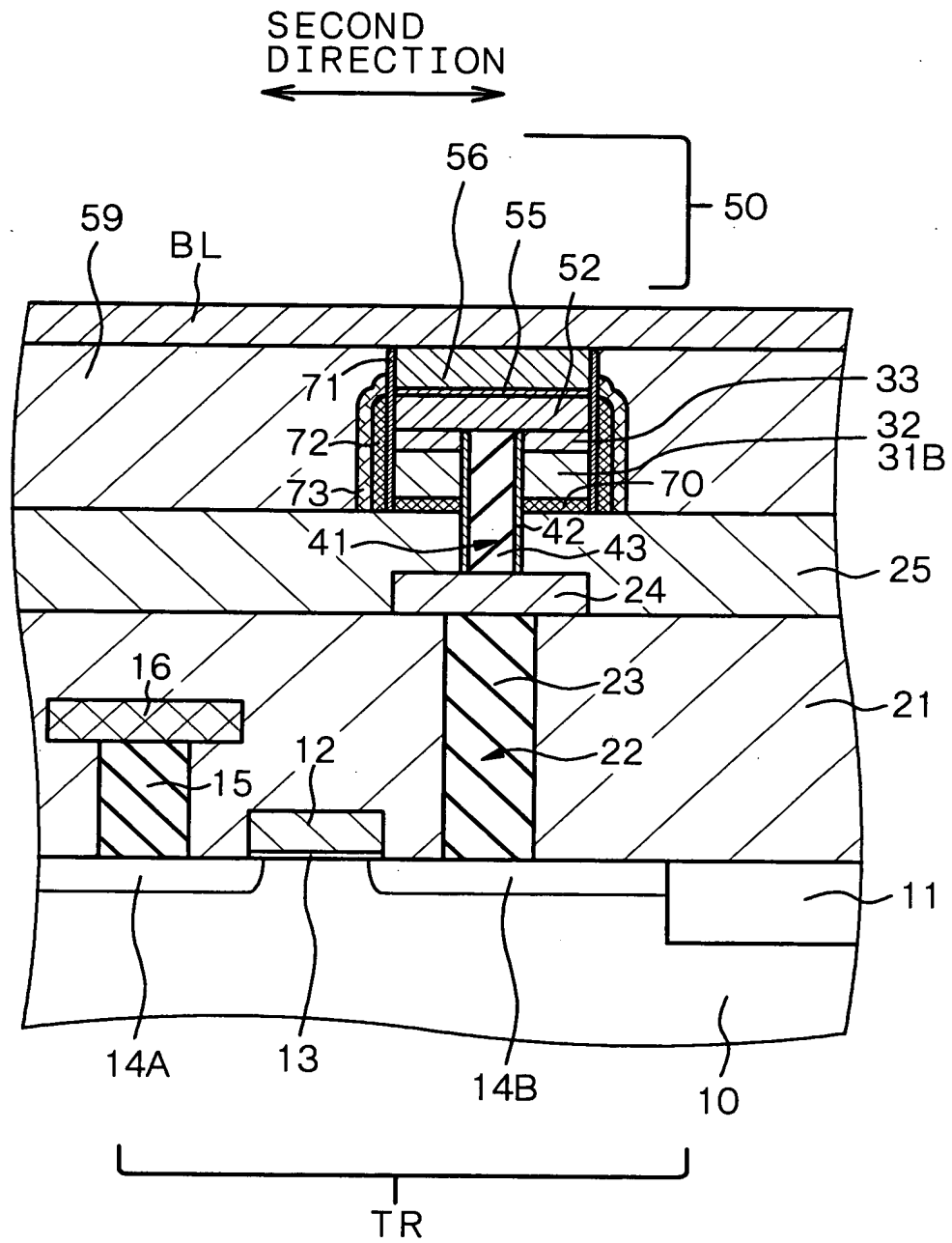
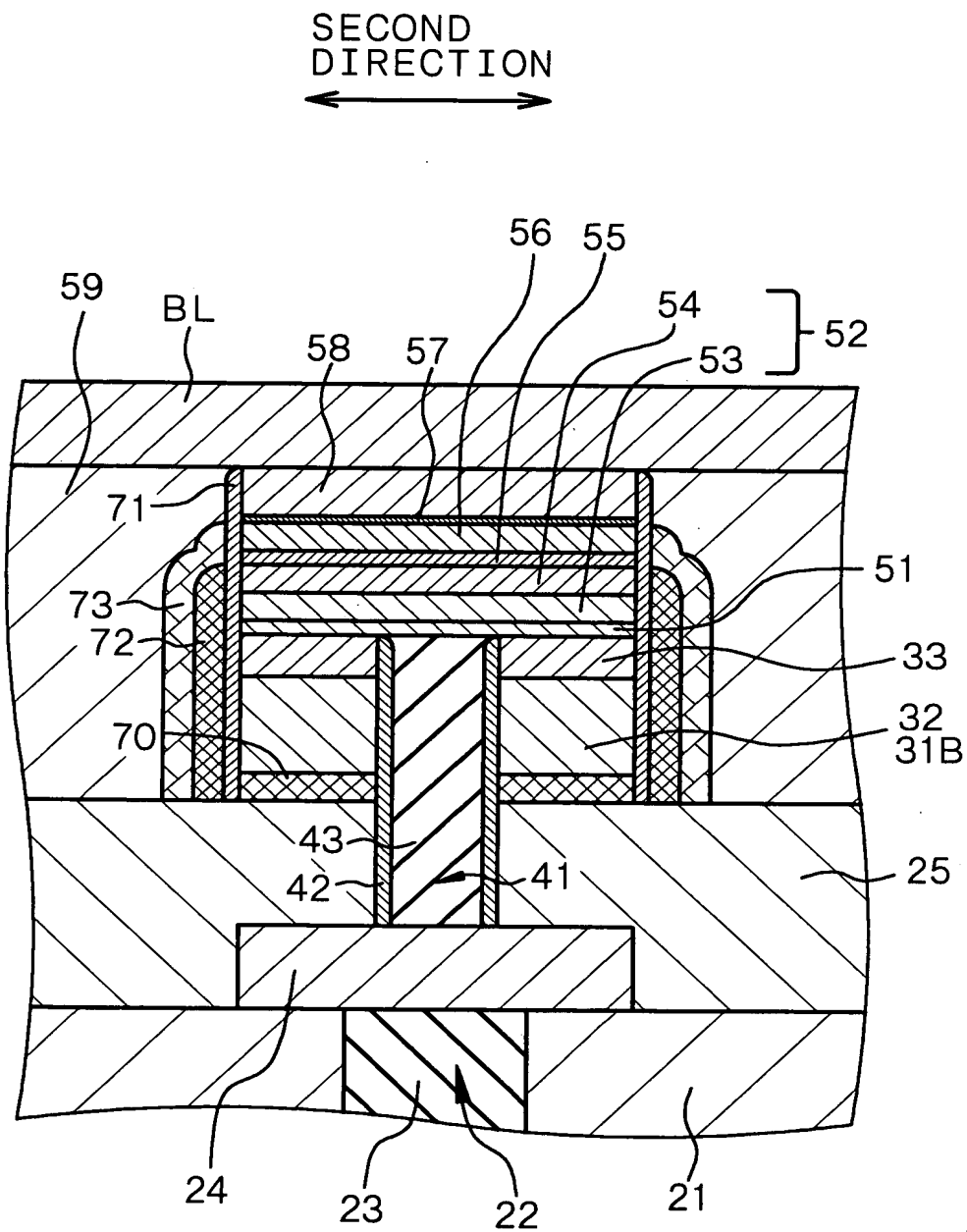
*Fig. 22*

Fig. 23



*Fig. 24*



*Fig. 25*

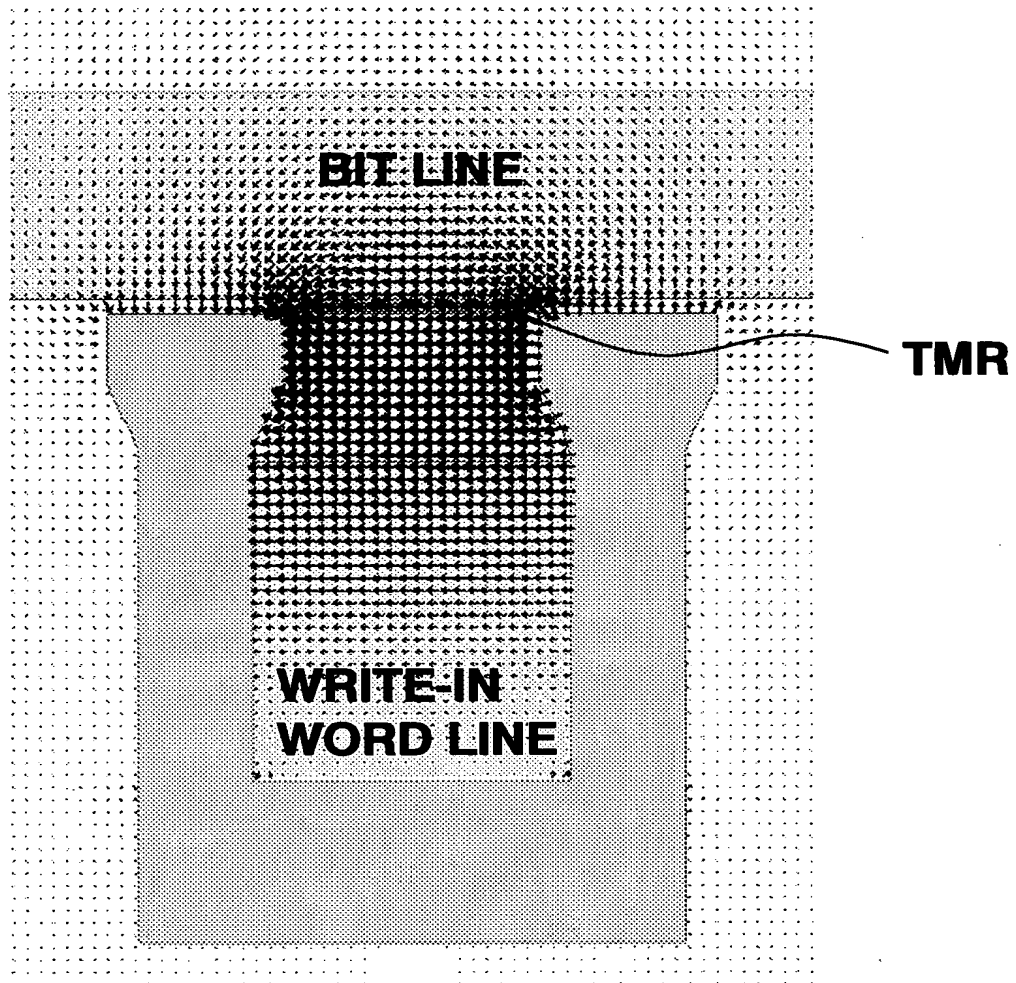


Fig. 26

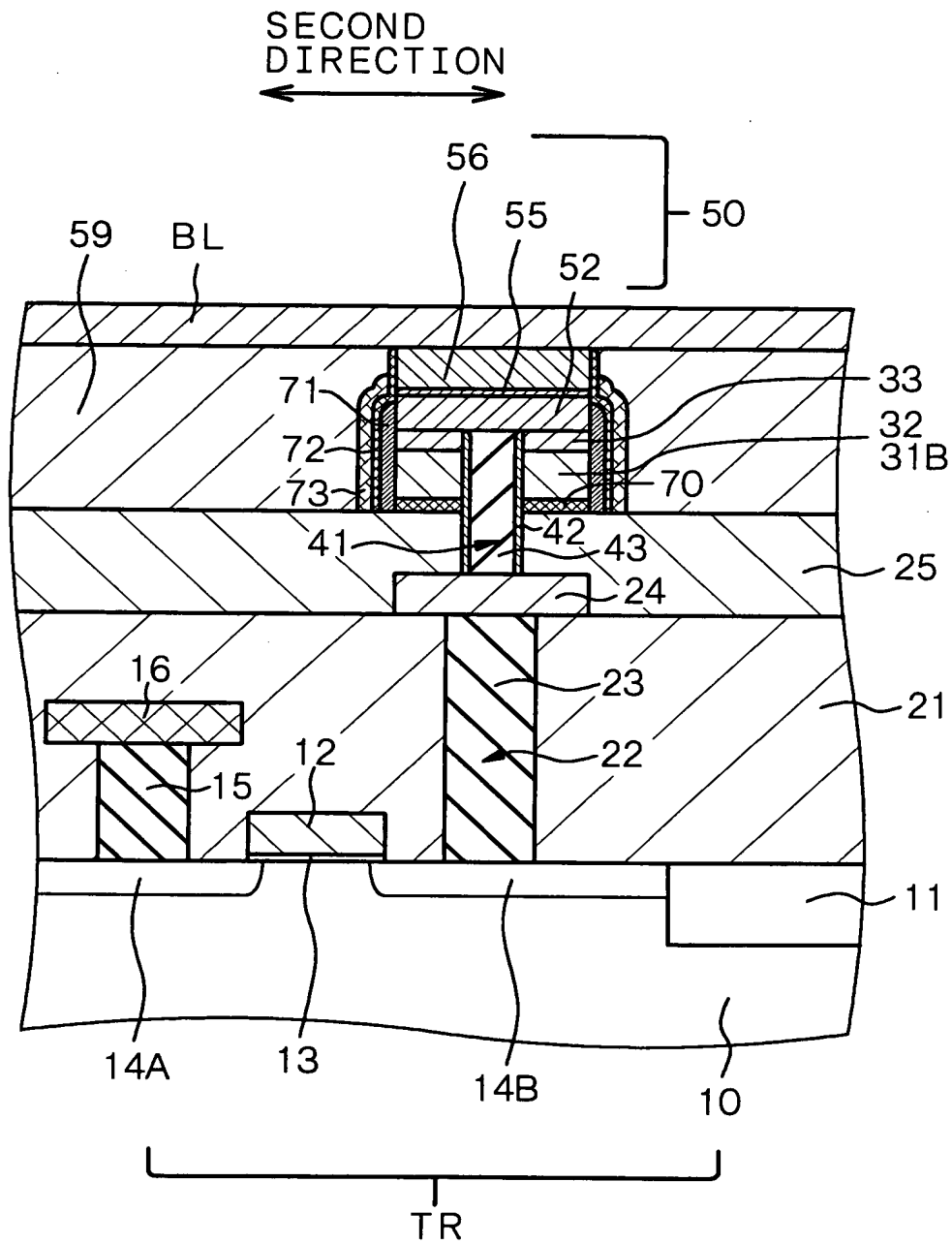


Fig. 27

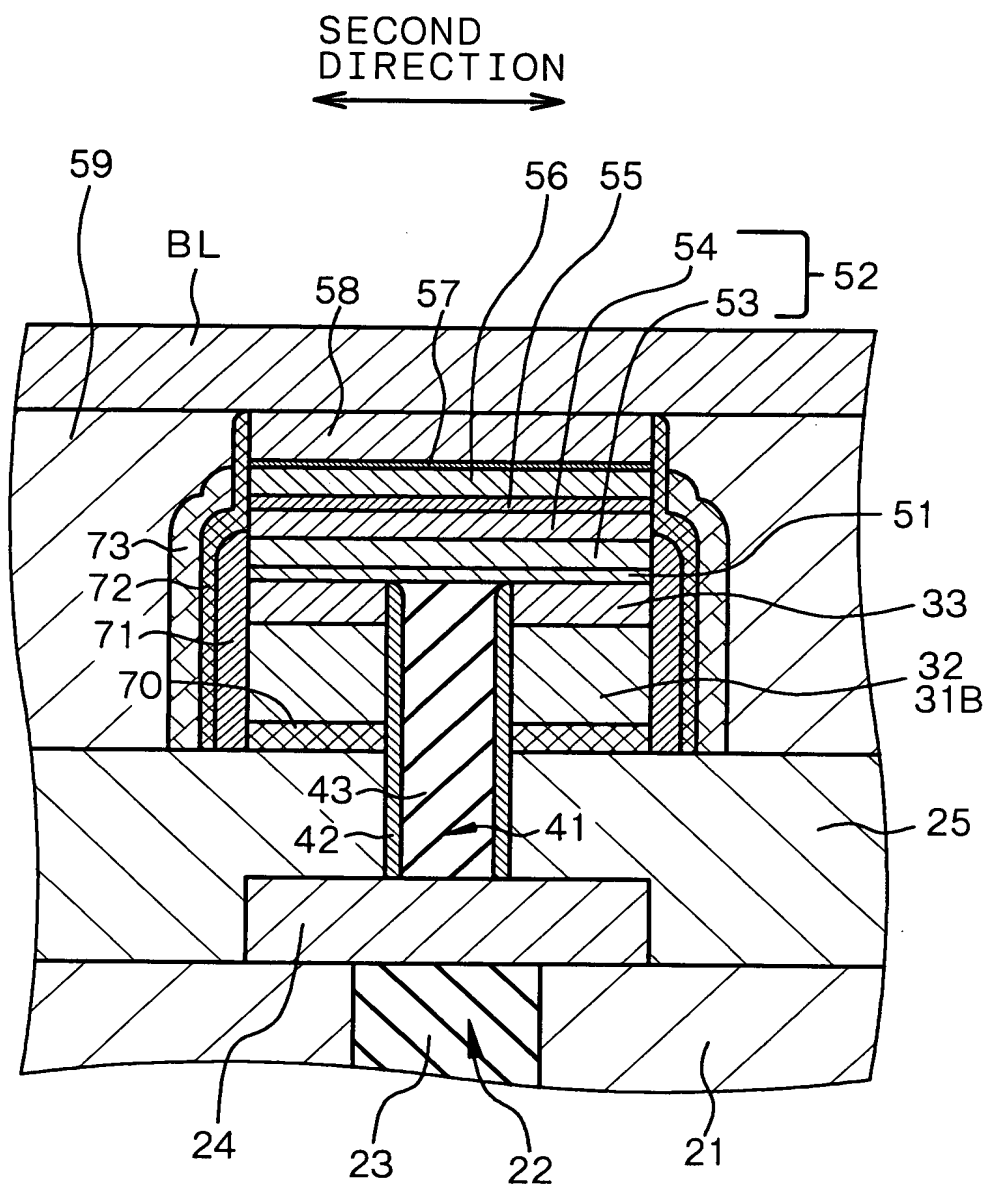


Fig. 28

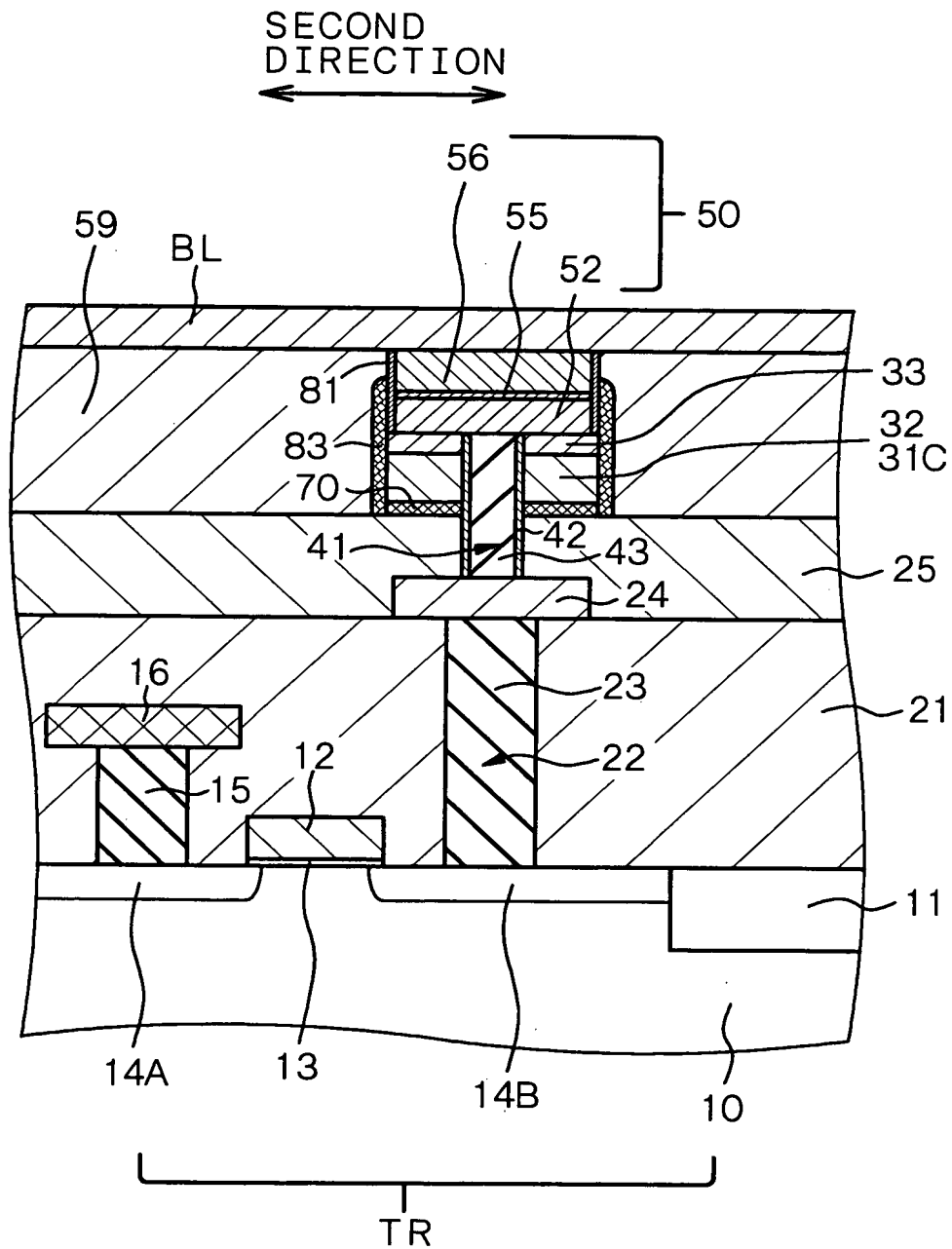
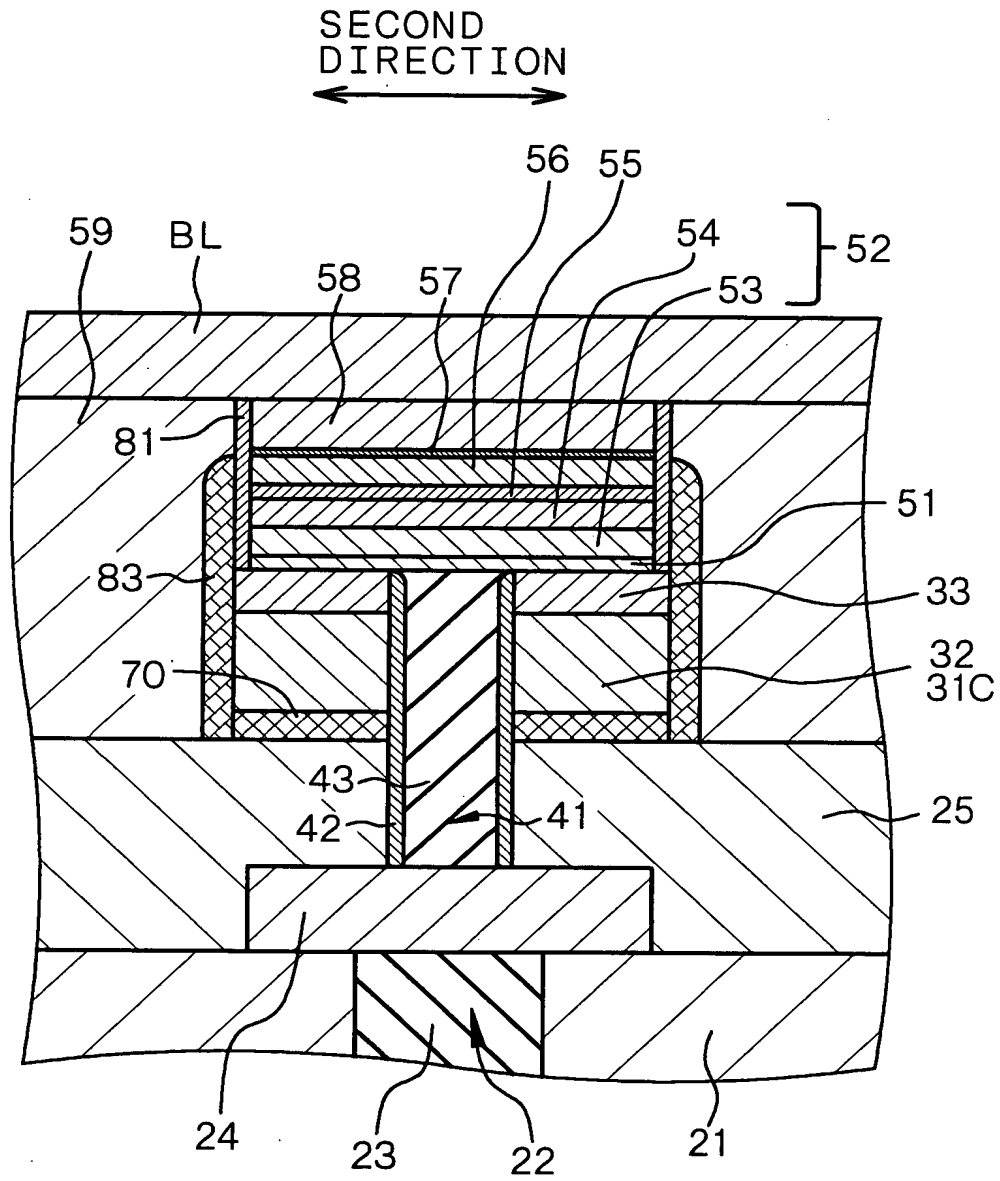
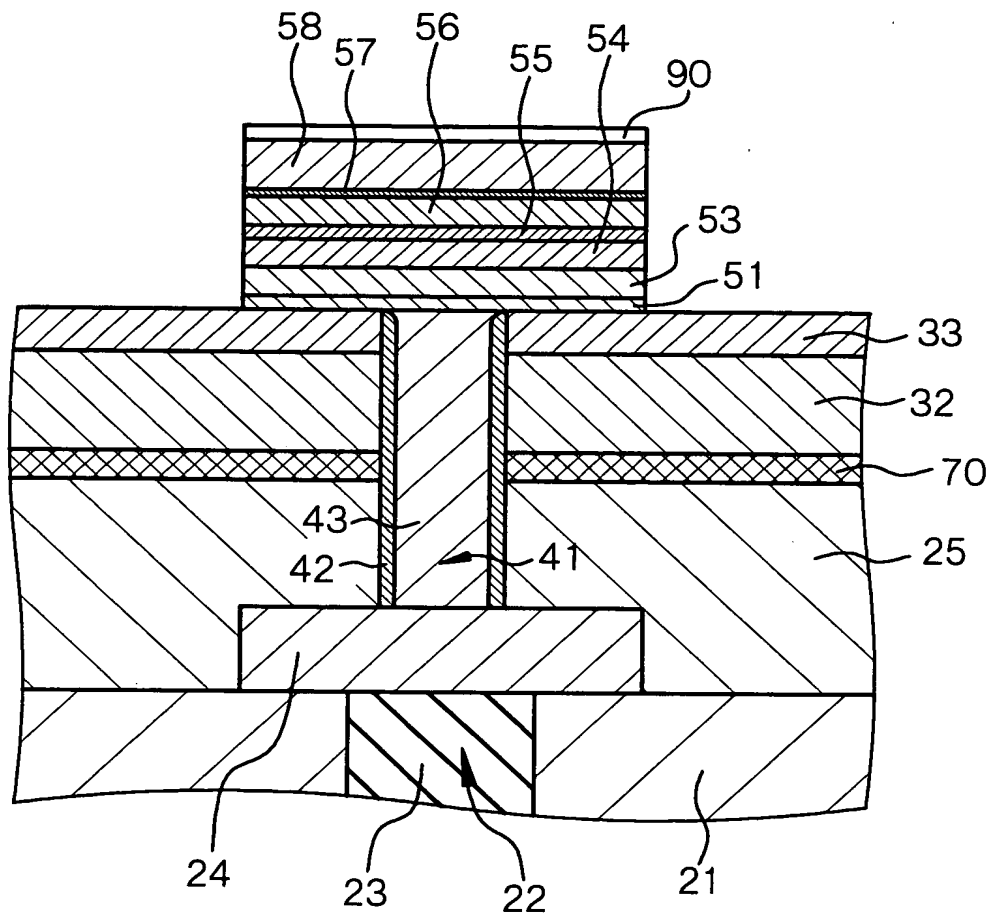


Fig. 29



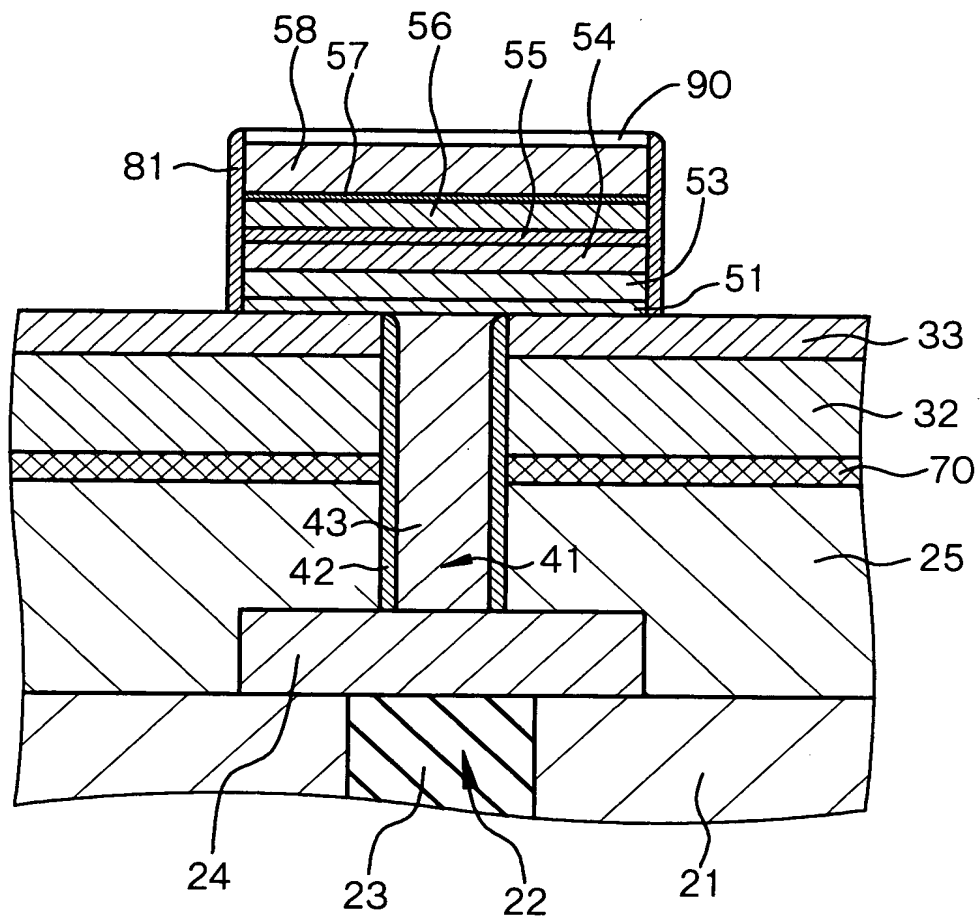
*Fig. 30*

[STEP-520]



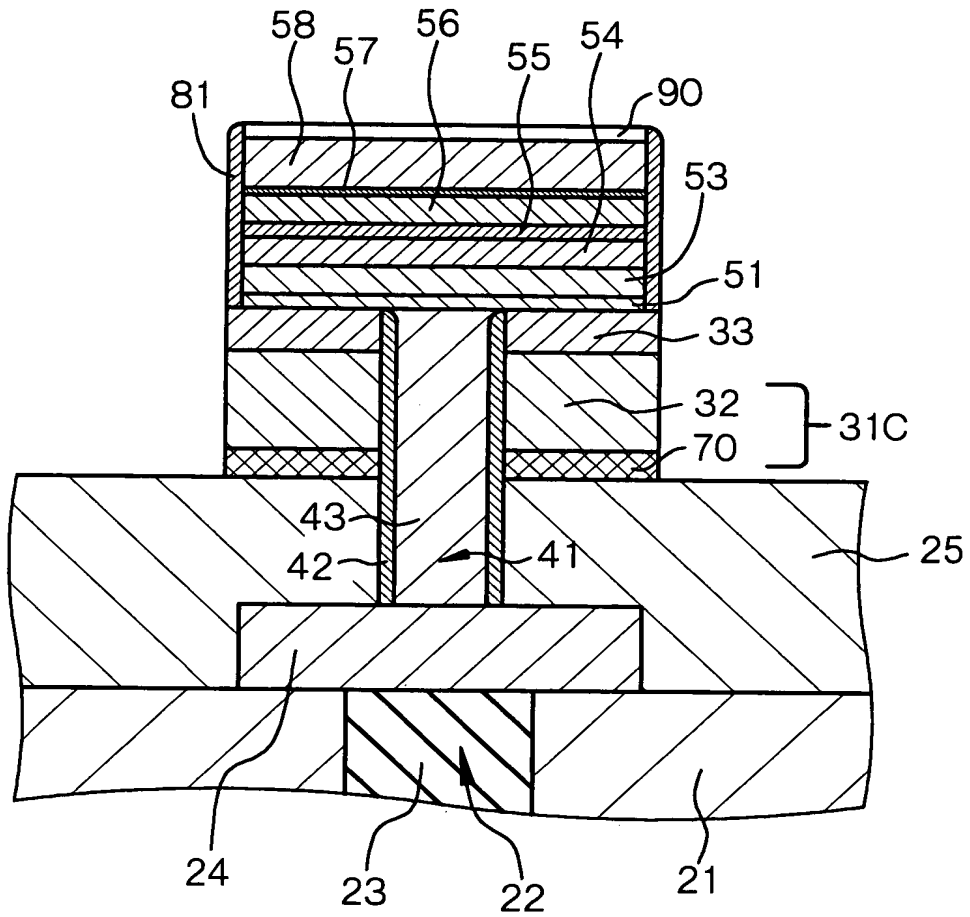
*Fig. 31*

[STEP-525]



*Fig. 32*

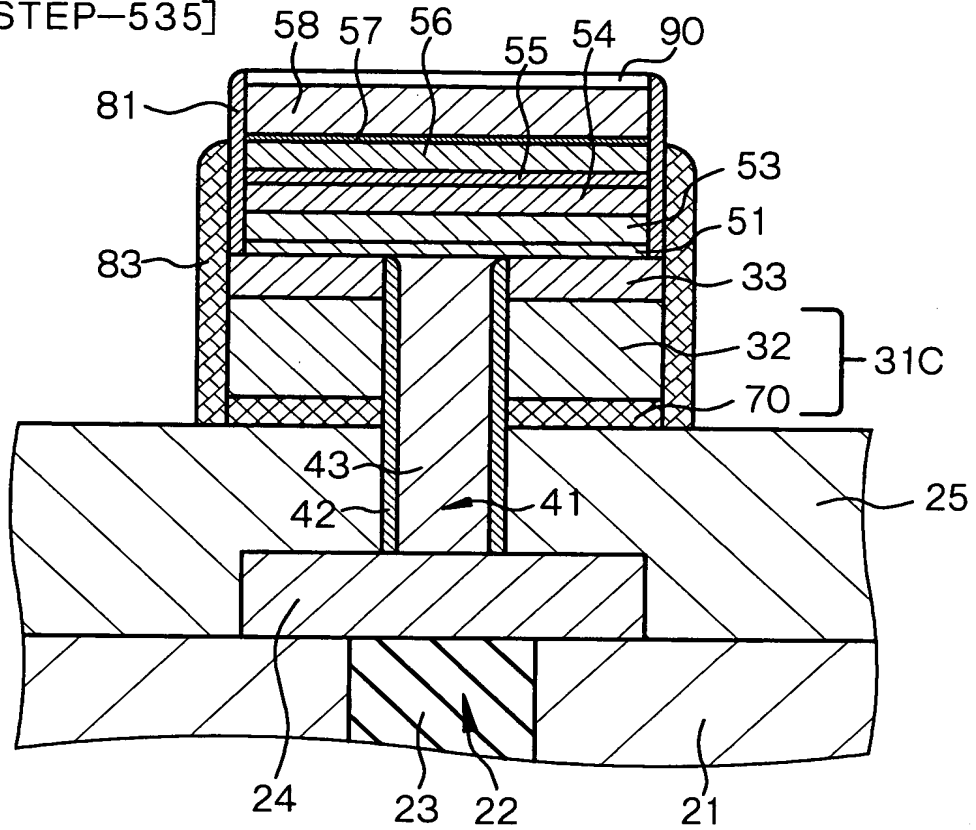
[STEP-530]



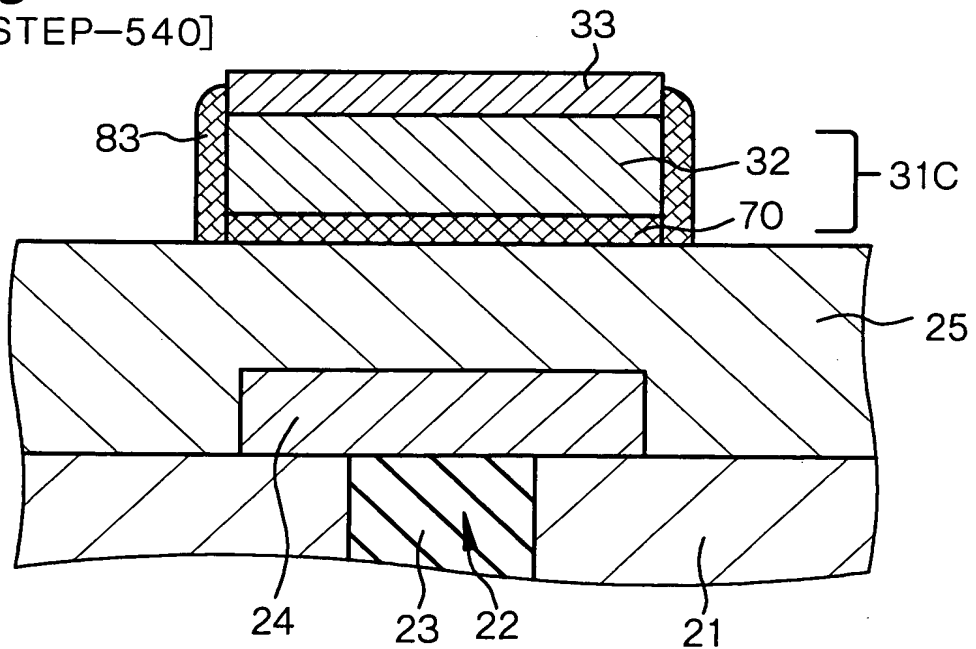


*Fig. 33A*

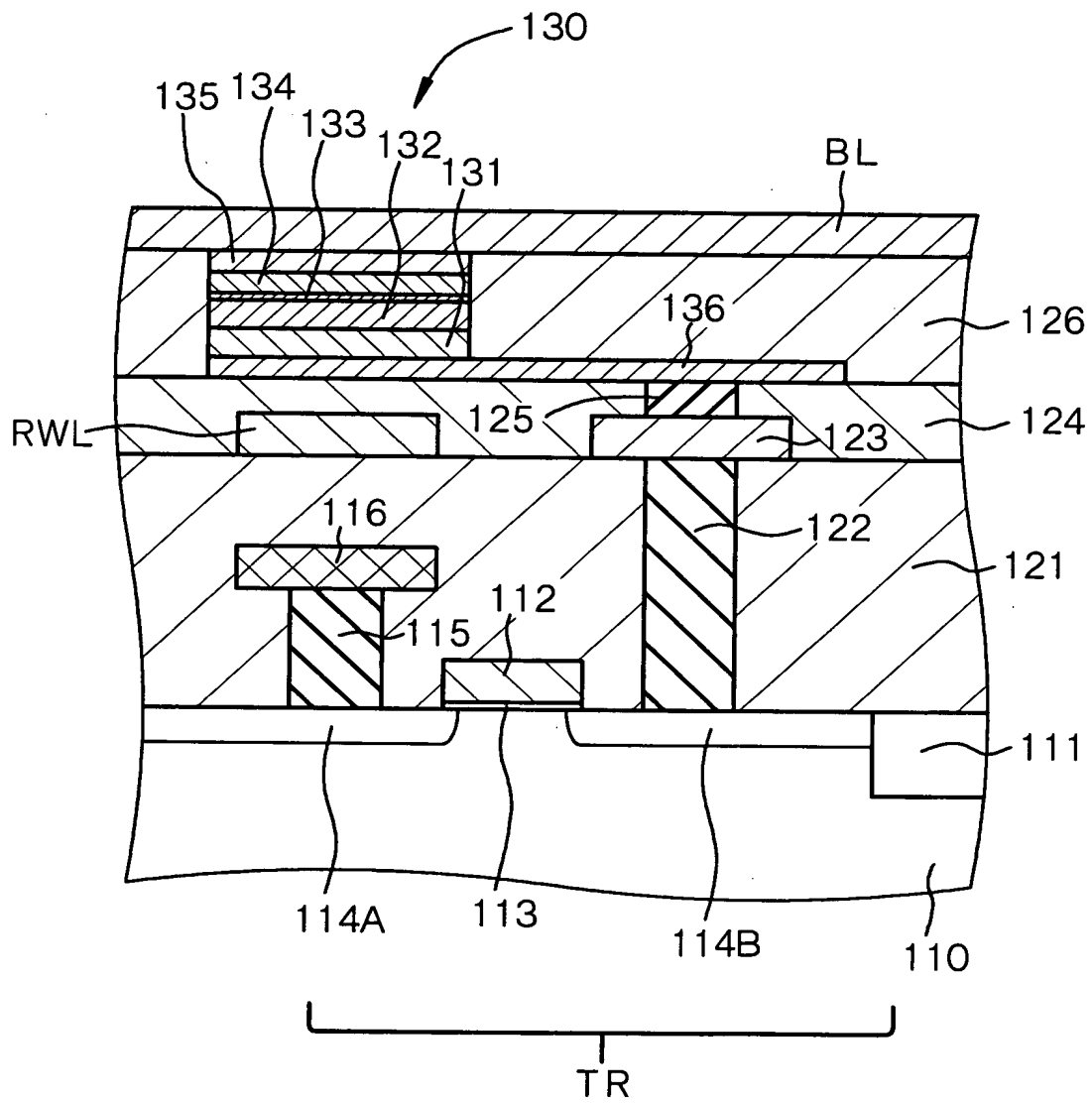
[STEP-535]

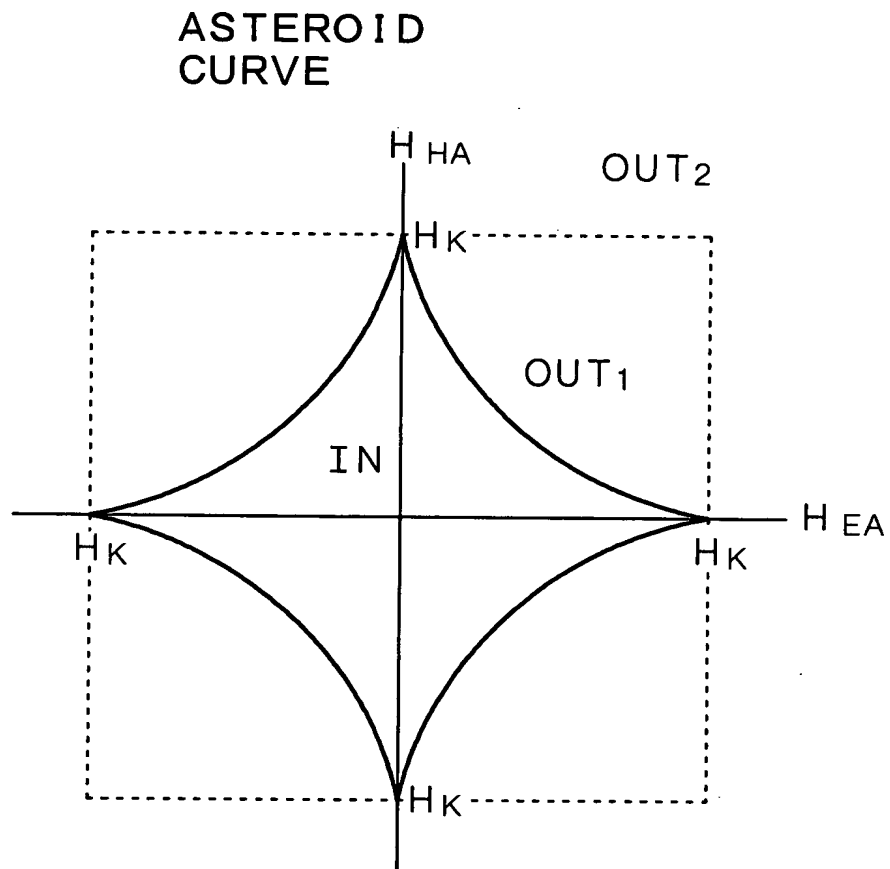
*Fig. 33B*

[STEP-540]

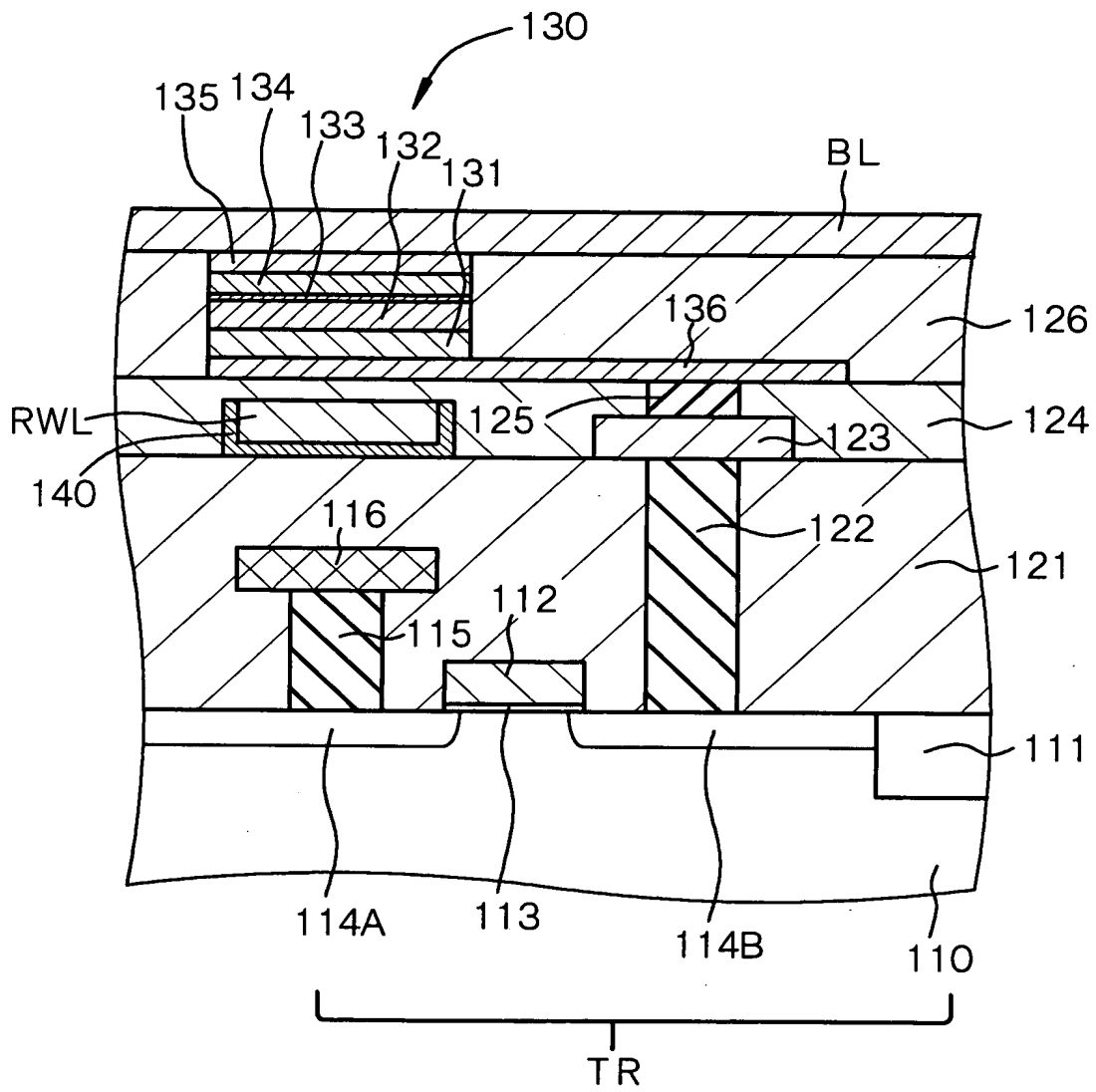


(PRIOR ART)

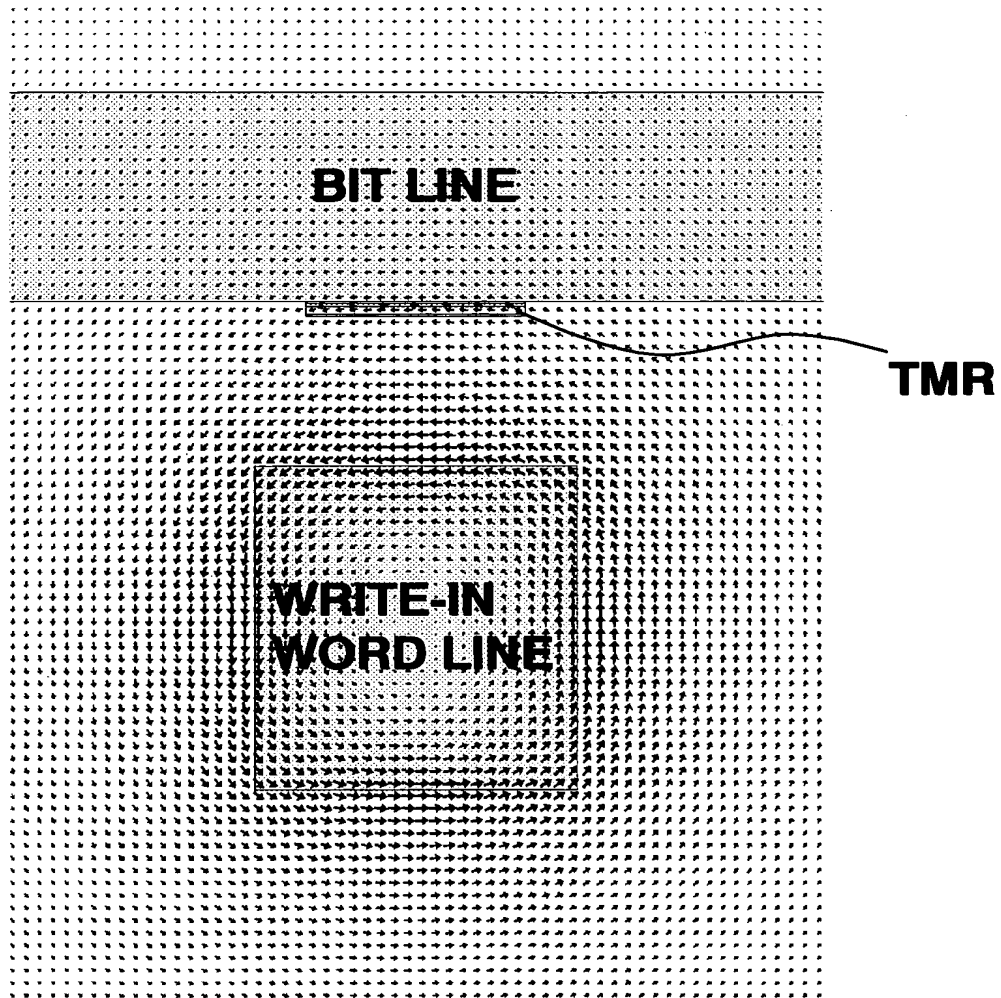


*Fig. 35*

(PRIOR ART)



*Fig. 37*



*Fig. 38*

